NYCU Computer Organization HW 7

1. Problems in this exercise refer to the following sequence of instructions, and assume that it is executed on a five-stage pipelined datapath

```
add     x15, x12, x11
lw      x13, 8(x15)
lw      x12, 0(x2)
or      x13, x15, x13
sw      x13, 0(x15)
```

   a. If there is no forwarding or hazard detection, insert NOPs to ensure correct execution.
   b. If the processor has forwarding, but we forget to implement the hazard detection unit, what happens when the original code executes?
   c. If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units.

Cycle	1	2	3	4	5	6	7	8
add	IF	ID	EX	ME	WB			
lw		IF	ID	EX	ME	WB		
lw			IF	ID	EX	ME	WB	
or				IF	ID	EX	ME	WB
sw					IF	ID	EX	ME

   Because there are no stalls in this code, PCWrite and IF/IDWrite are always 1 and the MUX before ID/EX is always set to pass the control values through
   Cycle 1 ForwardA = X; ForwardB = X (no instruction in EX stage yet)
   What is the ForwardA and FowwardB signal result from cycle 2 – 5?

2. We assume that the breakdown of dynamic instructions into various instruction categories is as follows.

R-Type	beqz/bnez	jal	lw	sw
40%	25%	5%	25%	5%

Also, we assume the following branch predictor accuracies

Always-Taken	Always-Not-Taken	2-Bit
45%	55%	85%

   a. What is the extra CPI due to mispredicted branches with the always-taken predictor? Assume that branch outcomes are determined in the ID stage and applied in the EX stage that there are no data hazard, and that no delay slots are used.

b. What is the extra CPI due to mispredicted branches with the 2-bit predictor?
c. Some branch instructions are much more predictable than others. If we know that 80% of all executed branch instructions are easy-to-predict loop-back branches that are always predicted correctly, what is the accuracy of the 2-bit predictor on the remaining 20% of the branch instructions?