NYCU Computer Organization HW 5

1. True or False: Any RISC-V datapath using edge-triggered writes must have more than one copy of the register file.
2. “Register read” is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. “Register setup” is the amount of time a register’s data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

IMEM/D-MEM	REG	MUX	ALU	Adder	Single gate	Register Read	Register Setup	Sign Extend	Control
250 ps	150 ps	25 ps	200 ps	150 ps	5 ps	30 ps	20 ps	50 ps	50 ps

   2.1 What is the latency of an R-type instruction (i.e. how long must the clock period be to ensure that this instruction works correctly)? The time unit of the latency is ps.

   2.2 What is the latency of lw?

   2.3 What is the latency of beq?