

NYCU Computer Organization HW 10

1. Increasing associativity requires more comparators and more tag bits per cache block. Assuming a cache of 4096 blocks, a four-word block size, and a 32-bit address, find the total number of sets and the total number of tag bits for cache that are direct-mapped, two-way and four-way set associative, and fully associative.
2. Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate of 4GHz. Assume a main memory access time of 100ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 2%. How much faster will the processor be if we add a secondary cache that has 5ns access time for either a hit of a miss and is large enough to reduce the miss rate to main memory to 0.5%?