National Yang Ming Chiao Tung University
Computer Architecture & System Lab

# Computer Organization

## Syllabus

Tsung Tai Yeh
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# Course Information

- Instructor: **Tsung Tai Yeh**
  - ttyeh@cs.nycu.edu.tw
- TA team+: (EC-619)
- Lecture: T2R56
- Course website
  - https://reurl.cc/jQ4mm2

Course website QR Code

# Course Information

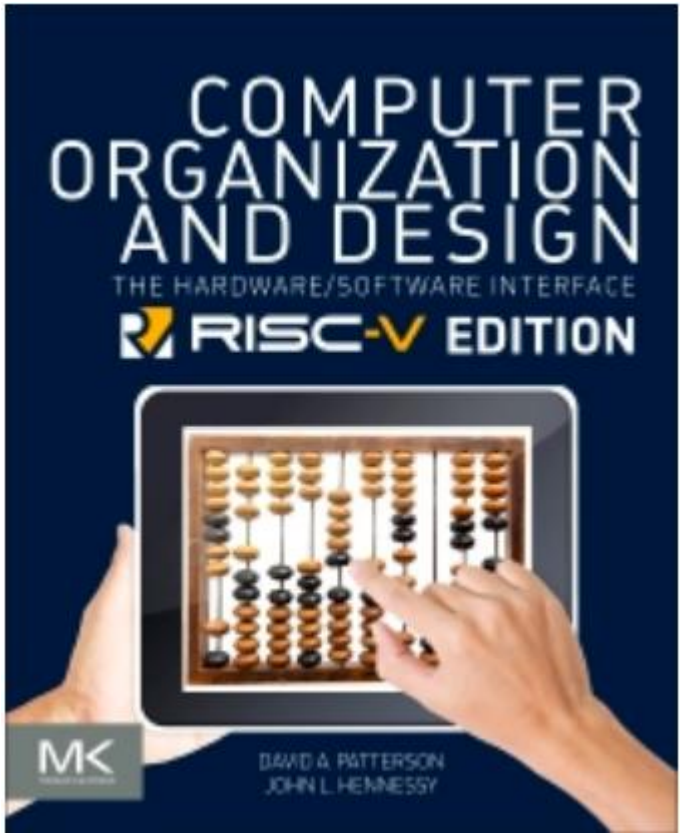
- **Lecture time:**
  - 9:00 - 9:50 am (Tue.) and 1:20 pm - 3:10 pm (Thur.)
- **Classroom:** EC-115
- **Grade:**
  - 45% for 4 lab assignments, 25% midterm, and 30% final exam
  - Midterm exam: 4/10 during the class
  - Final exam: 6/5 during the class

# Intended Lecture Outcomes (ILOs)

- Learn the great ideas of computer organization
- Learn the formats of the RISC-V **instruction set**
- Understand the details of the **pipelining CPU** processor organization
- Introduce the **memory hierarchies** (DRAM and Cache)
- Implement a simple RISC-V CPU processor

# Textbook

- Computer Organization and Design, RISC-V Edition: The Hardware/ Software Interface, 2017
  - John L. Hennessy and David A. Patterson



# Lecture Topics

- RISC-V Instruction Set Architecture (ISA)
- CPU Processor Organization
  - Pipelining
  - Branch prediction
  - Multi-core
- Memory Hierarchy
  - DRAM Memory
  - Cache Organization

# Prerequisite Courses

- Prerequisite Courses
  - Digital Circuit Design
  - Data Structures and Object-oriented Programming
- Prerequisite Techniques
  - C/C++ Programming
  - Verilog Programming

# Lab Assignments

- 4 lab assignments
- Need to use Verilog and Python to do each lab assignment
- Please submit your code to E3 by the deadline
- You can ask questions via discord
- https://discord.gg/srDSqpX8CJ
- Late submit penalty: cut 10% score of that lab per week

# Lab Assignments

- Lab 0 (for practice)
  - Environment Setup & simple Verilog practice
- Lab 1 (10%, submission deadline: 3/20)
  - Single Cycle CPU w/ Simple RISC-V Instruction
- Lab 2 (10%, submission deadline: 4/10)
  - Single Cycle CPU w/ Branch Instruction
- Lab 3 (10%, submission deadline: 5/1)
  - Simple Pipeline CPU
- Lab 4 (15%, submission deadline: 5/22)
  - Advance Pipeline CPU
- Lab 5 (optional)
- Implement Cache Manager