PHISON

Advanced

FW Concepts

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AGENDA

- Recap
- Read Errors
- Read Disturbance
- Rebuild
- Bad Block Management
- Wear Leveling
- Summary

Recap

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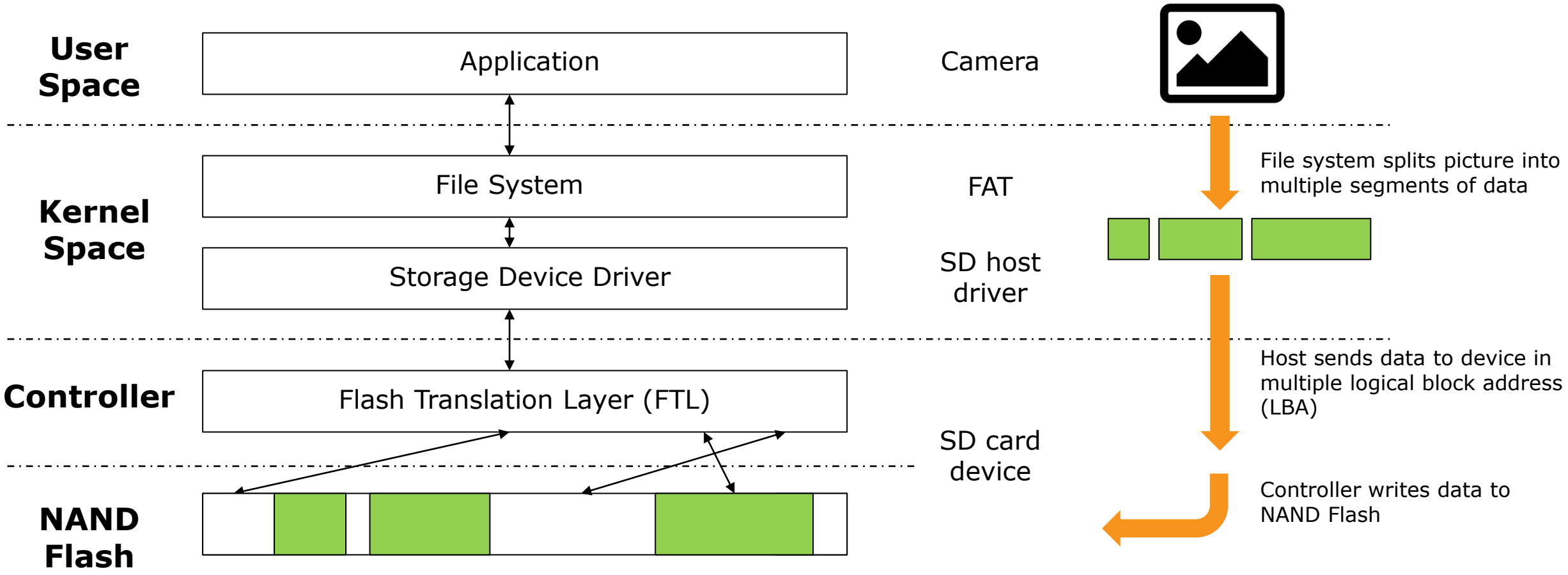
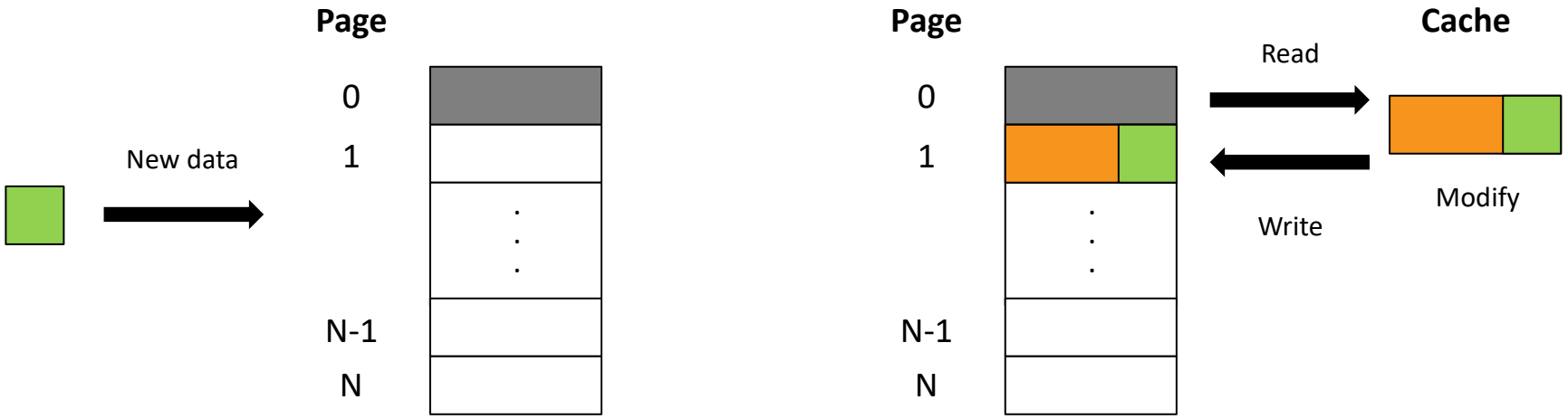
Application & Flash Storage Device



NAND Flash Limitations

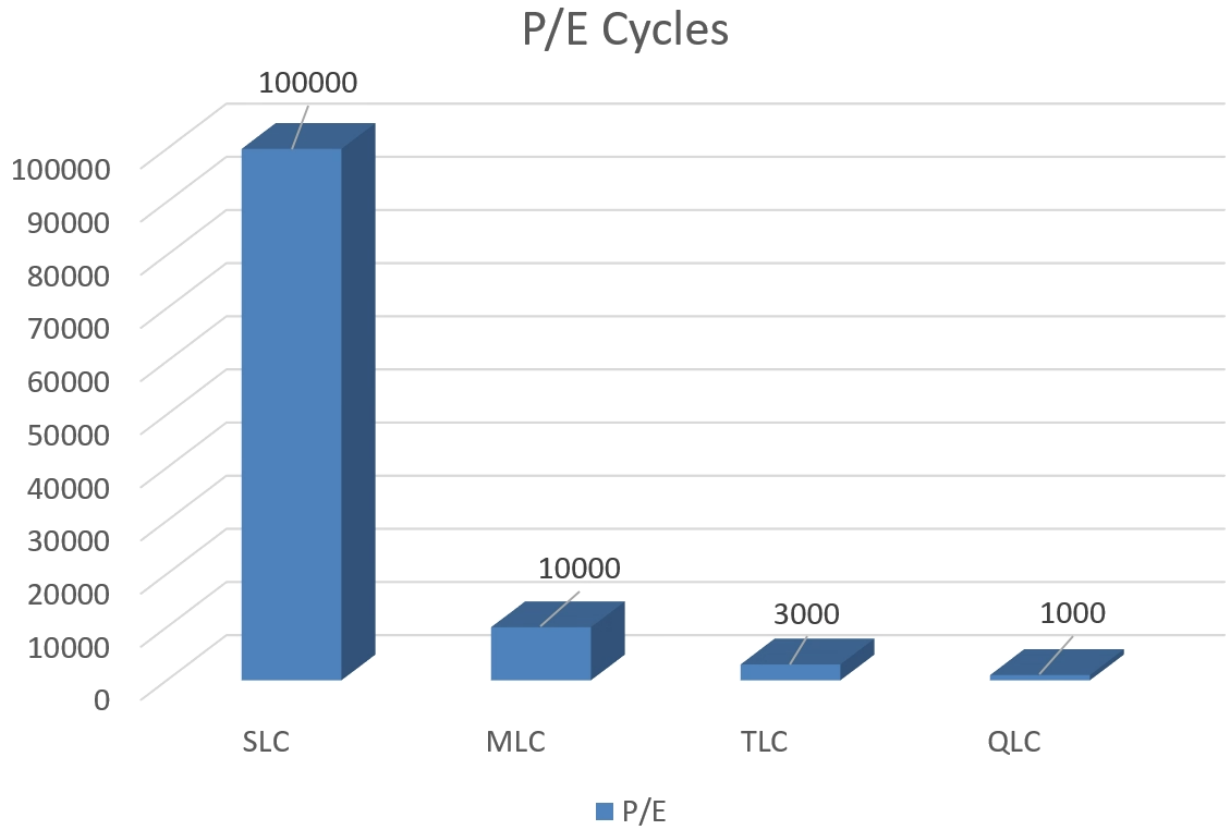
- **Page** is the smallest unit for read and program
- **Block** is the smallest unit for erase
- Must erase before program (cannot overwrite)



- Each read/program/erase operation has busy time to complete

NAND Flash Limitations

- Program/Erase (PE) Cycle: SLC = 100k, MLC = 10k, TLC = 3k
- Initial and runtime bad blocks
- Read errors & disturbance



Page Base vs Block Base

	Page Base	Block Base
Mapping Unit	Page (or 4KB)	Block
Table Size	Large (store in NAND Flash)	Small (store in SRAM)
R/W Performance	Excellent random write performance	Slow random write performance, but impressive read performance
Garbage Collection	Collect valid nodes when empty block becomes insufficient	Collect valid nodes when overwrite previous data or erase data
WAF	Low (efficient block utilization)	High (expensive merge operation)

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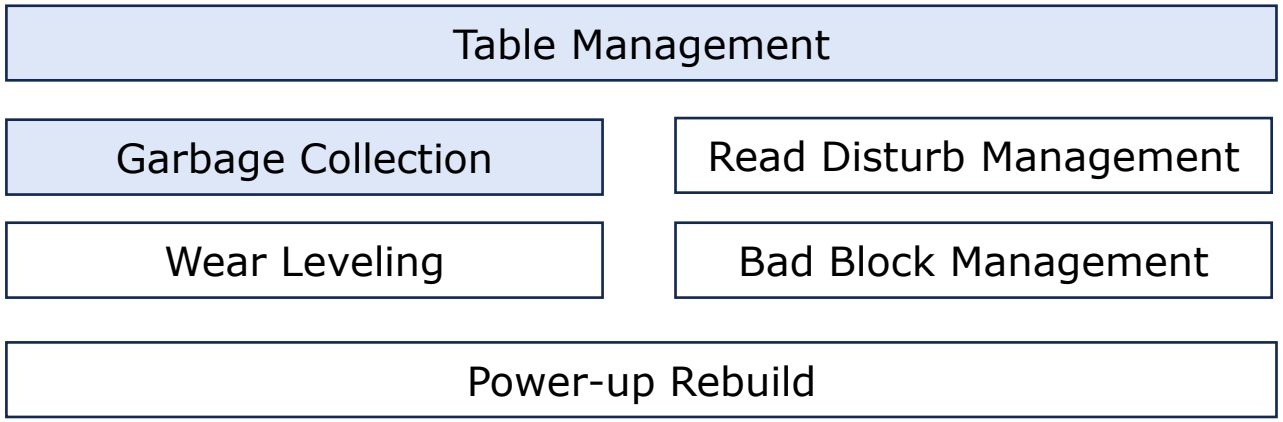
Table Management
Garbage Collection
Read Disturb Management
Wear Leveling
Bad Block Management
Power-up Rebuild

Read Errors

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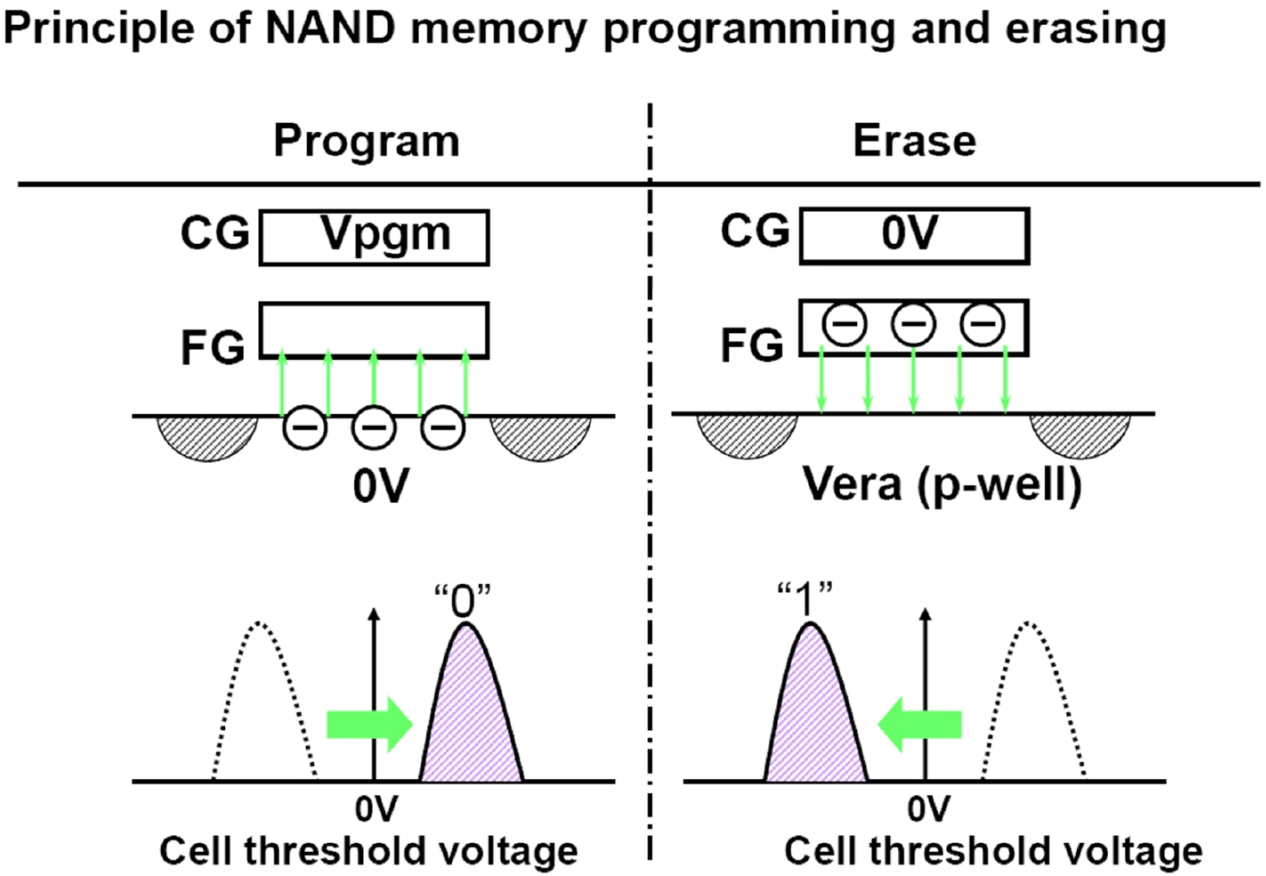
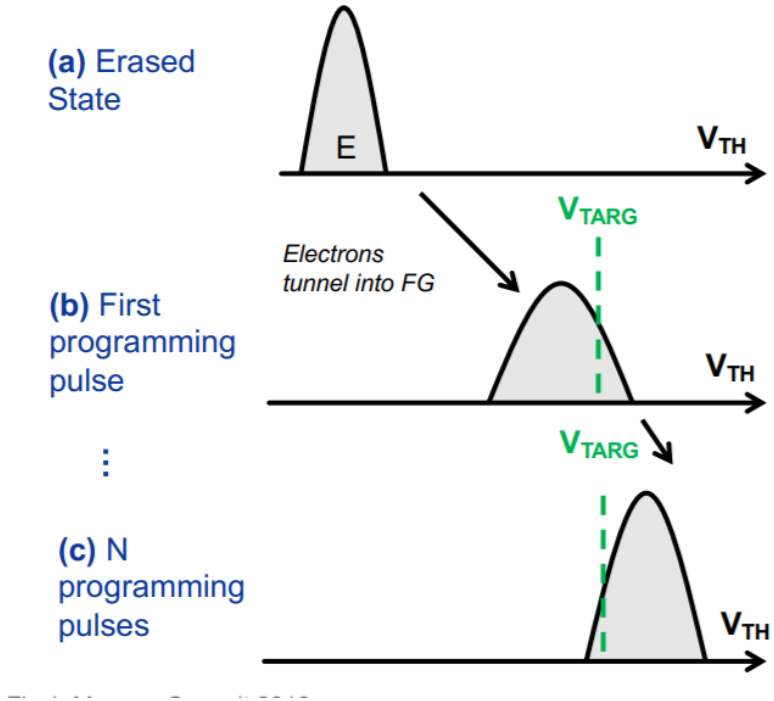
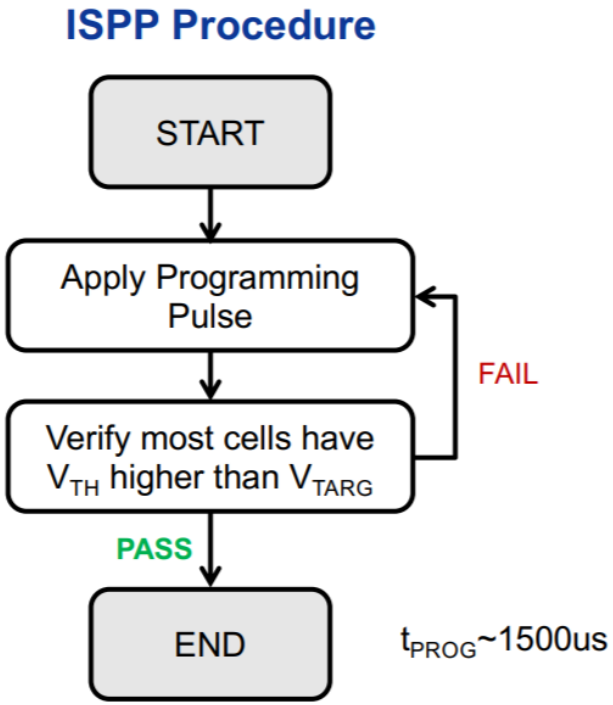
Program & Erase (P/E) Operation



Incremental Programming in NAND Flash

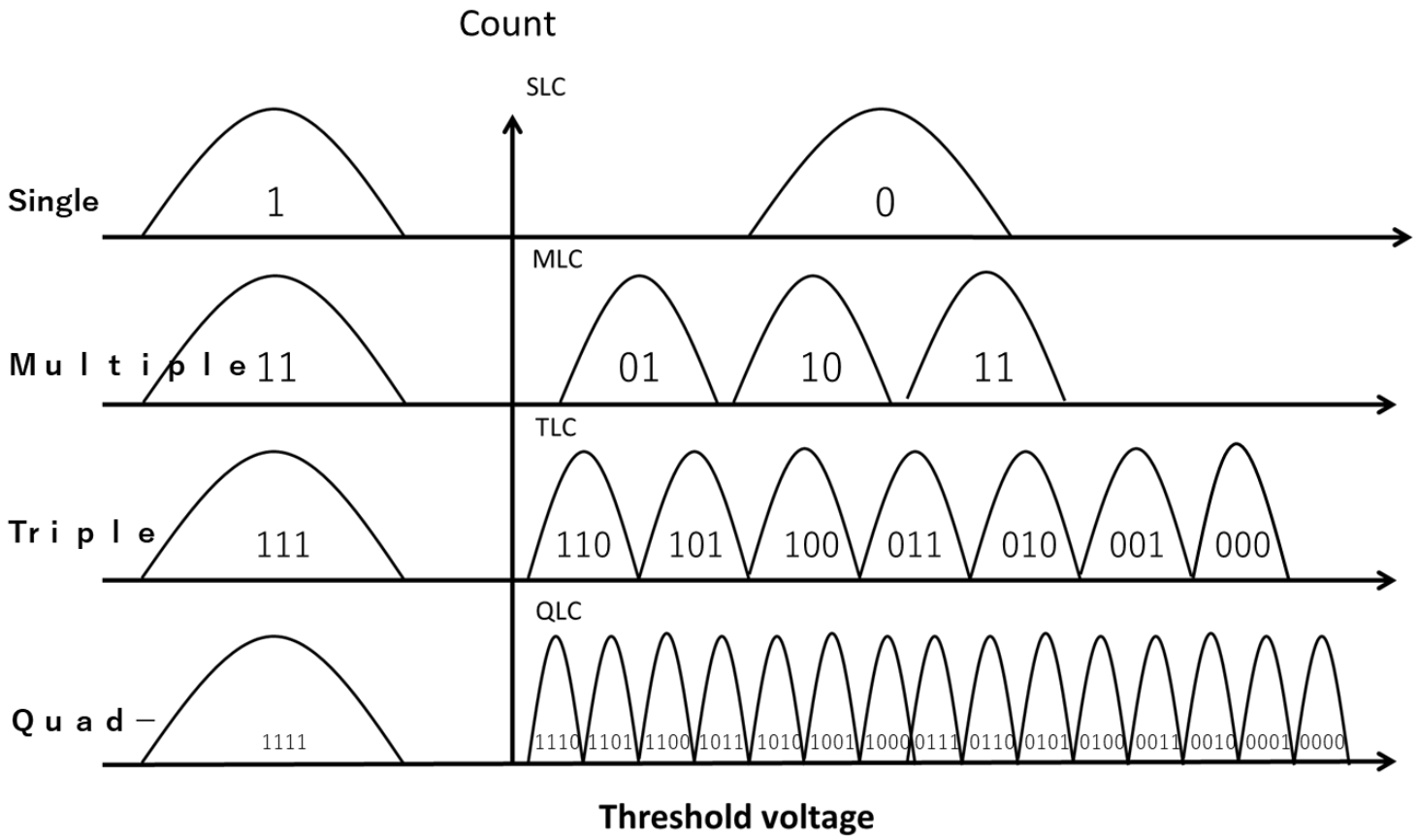
- VT shift changes from erased state to programmed state through incremental programming





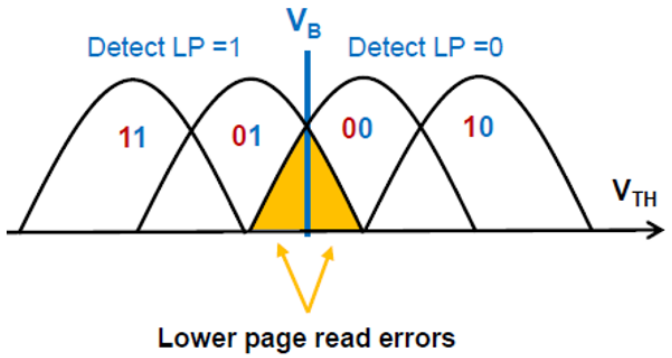
SLC vs MLC vs TLC

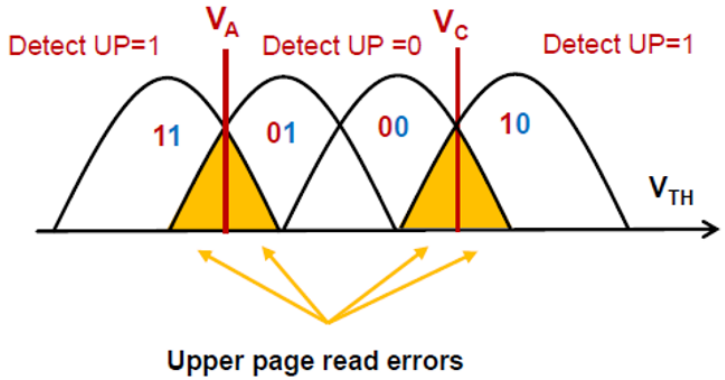
- Normal Voltage Threshold (VT) distribution



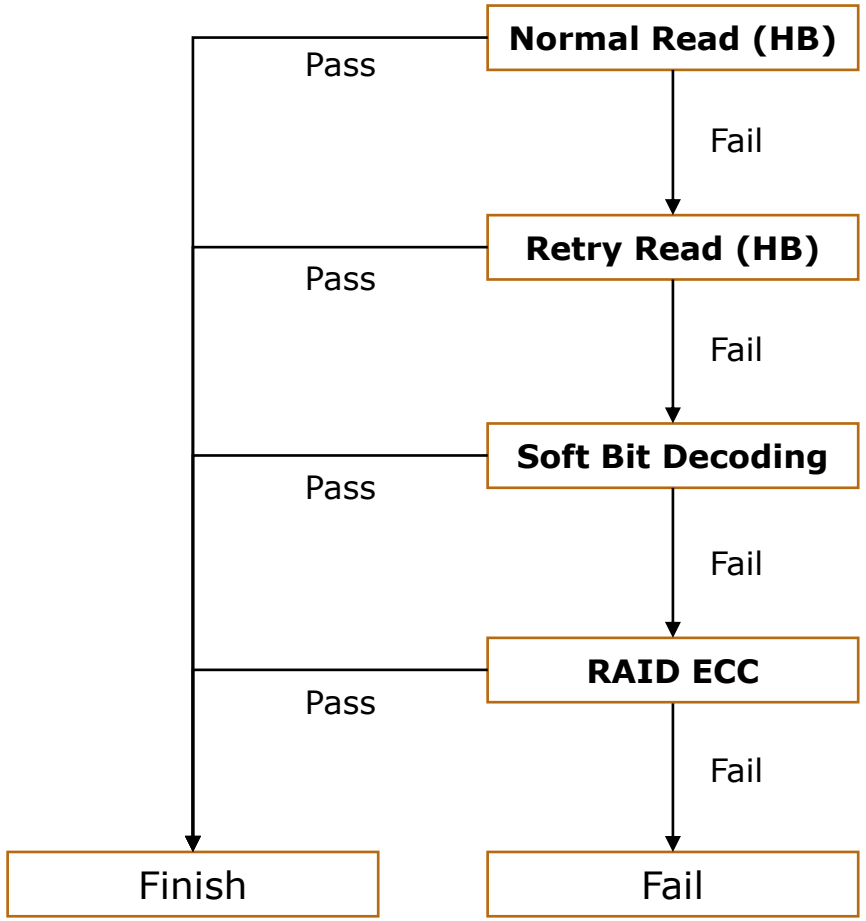
Read Errors

- Main sources of noise that would cause abnormal Vth distribution and read errors:
  - **Program/Erase cycling stress**: Program/erase pulses lead to degraded reliability of the underlying NAND flash cells.
  - **Cell-to-cell interference**: Threshold voltage of 'victim' cell is strongly affected by programming of neighboring 'aggressor' cells.
  - **Data retention**: Over time, electrons can escape from the programmed flash cells, causing a loss of threshold voltage.
  - **Read disturbance**: When reading a particular page in a block of NAND flash, a voltage is applied to all other WL in order to 'deselect' them. This applied voltage can affect the Vth distribution of the unselected WLs.



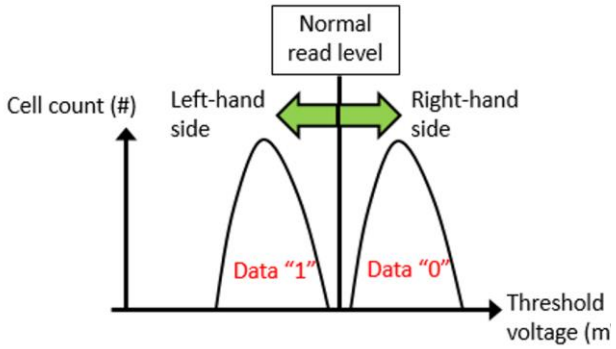


Error Handling Flow

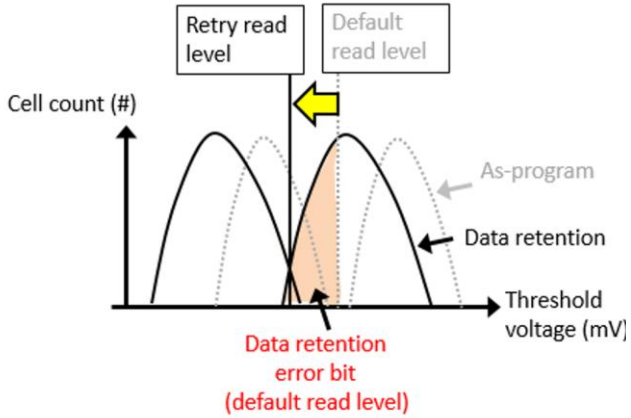


Error Handling Flow

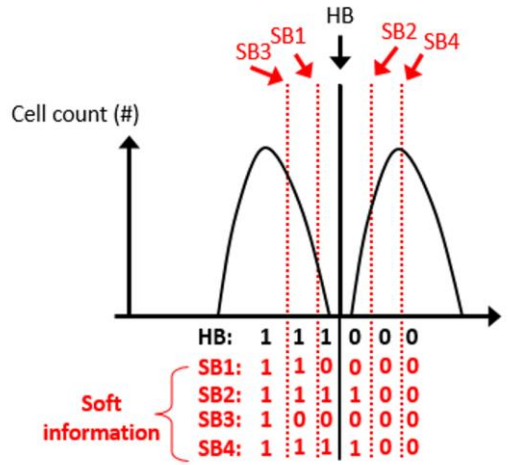
Normal Read



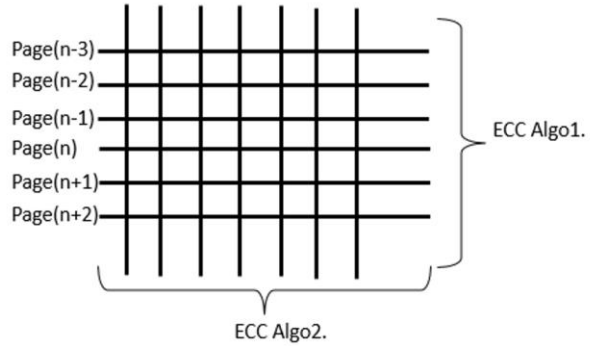
Read Retry



Soft Bit Decoding



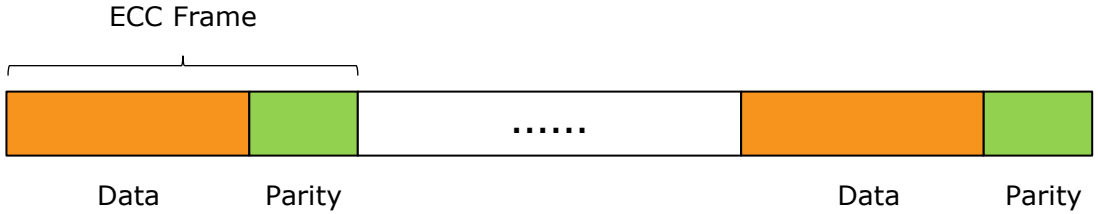
RAID ECC



Action: Read Page(n) data
1. When Page(n) ECC Algo1. decode fail
2. Read others page and decode with ECC Algo2. and interactive with Algo1.

Error Correction Codes (ECC)

- ECC Frame



- Phison ECC algorithms
  - BCH (Bose, Chaudhuri, Hocquenghem Algorithm)
  - BTC (Block Turbo Code)
  - LDPC (Low Density Parity Check)

Read Disturbance (RD)

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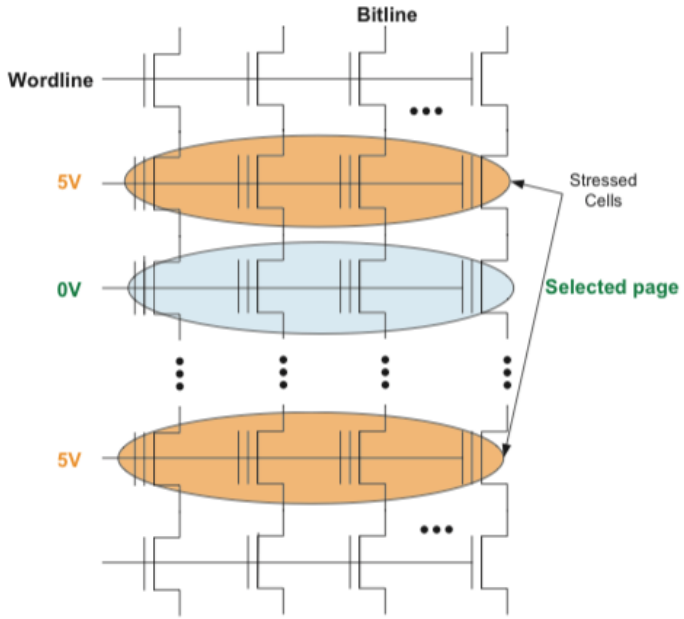
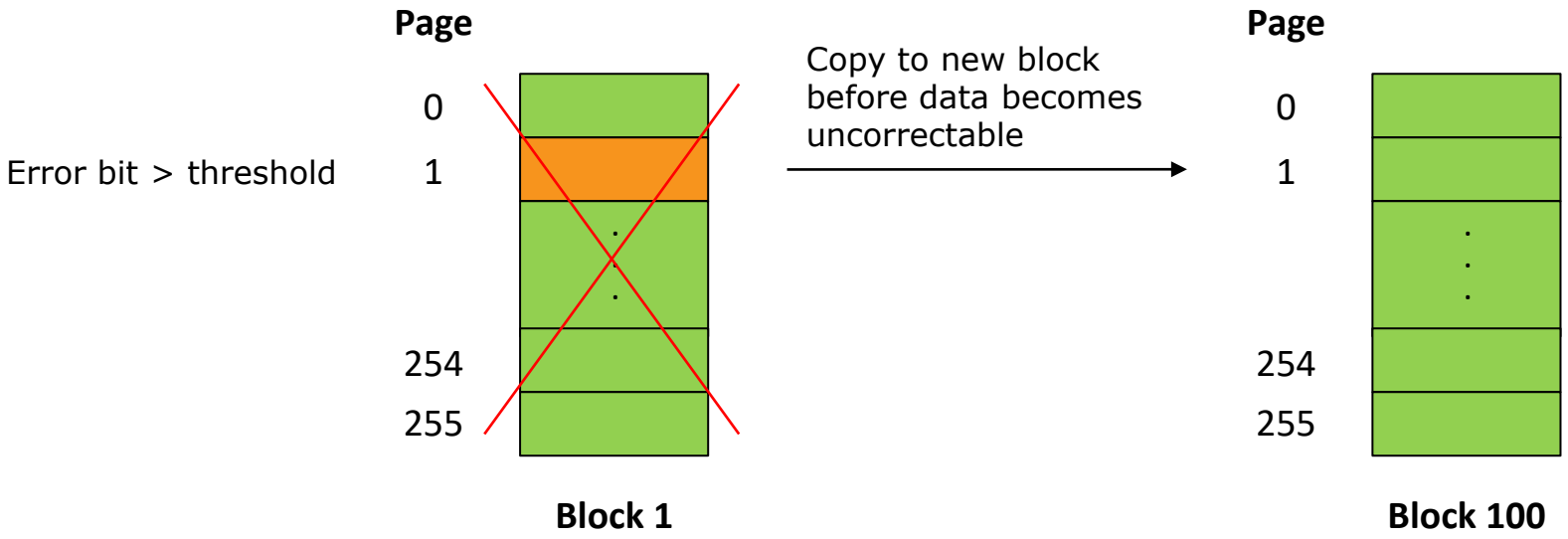
Background

- Read disturb occurs when the neighboring cells that are not being read receive elevated voltage stress
- They tend to be disturbed and move into a different logical state
- Some important system blocks such as FW code and mapping tables that are being read frequently would likely be affected and cause system failure



Solution

- Refresh block when exceed error bit threshold



- But the neighboring pages might have more serious disturbance than the page being read?
- How can we detect such read disturbance earlier?

Rebuild

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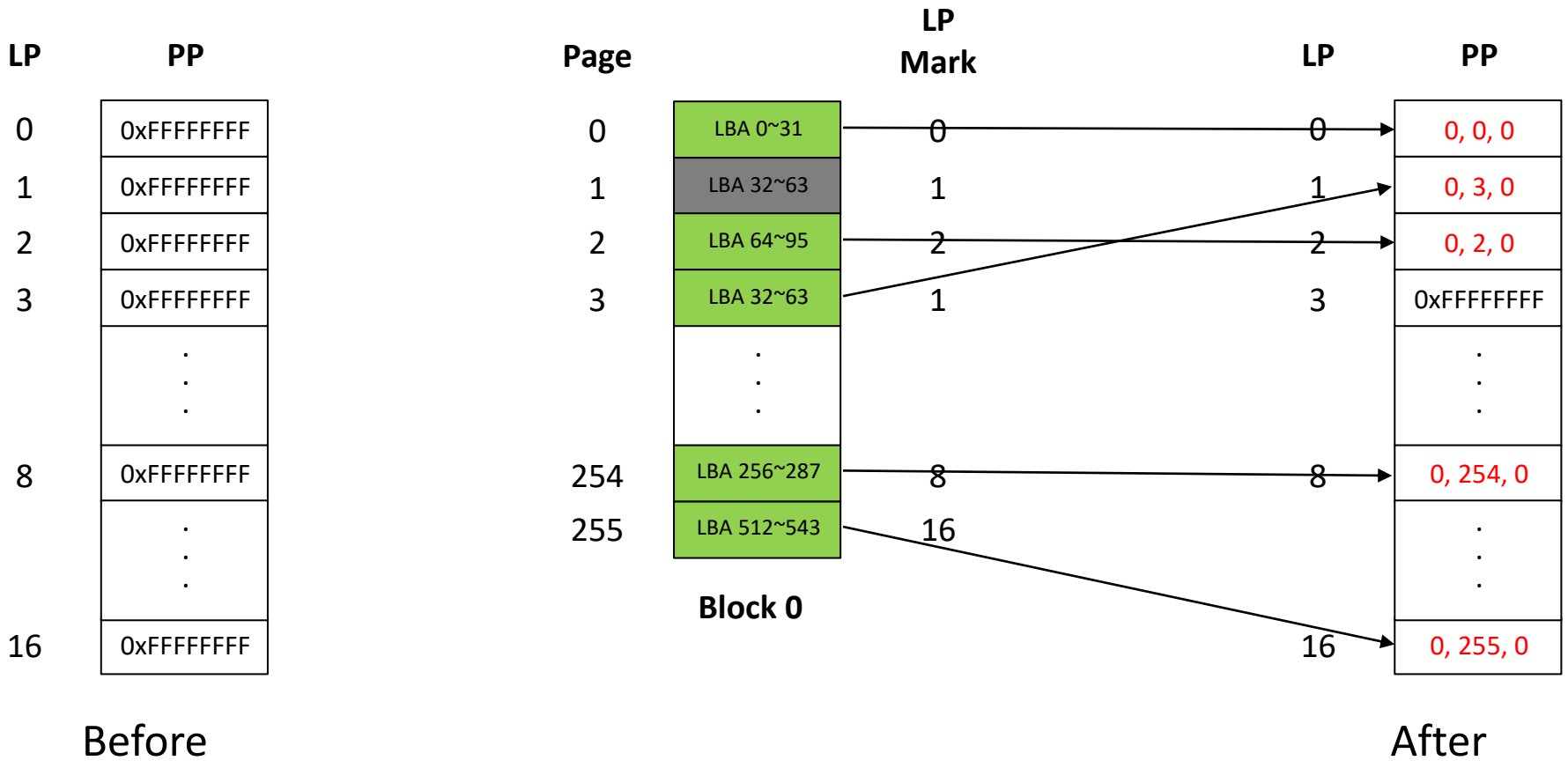
Sudden Power Loss

- Two main problems when Sudden Power Loss (SPL) occurs
  - Mapping table on SRAM is cleared
  - Not sure which page has been programmed in NAND Flash

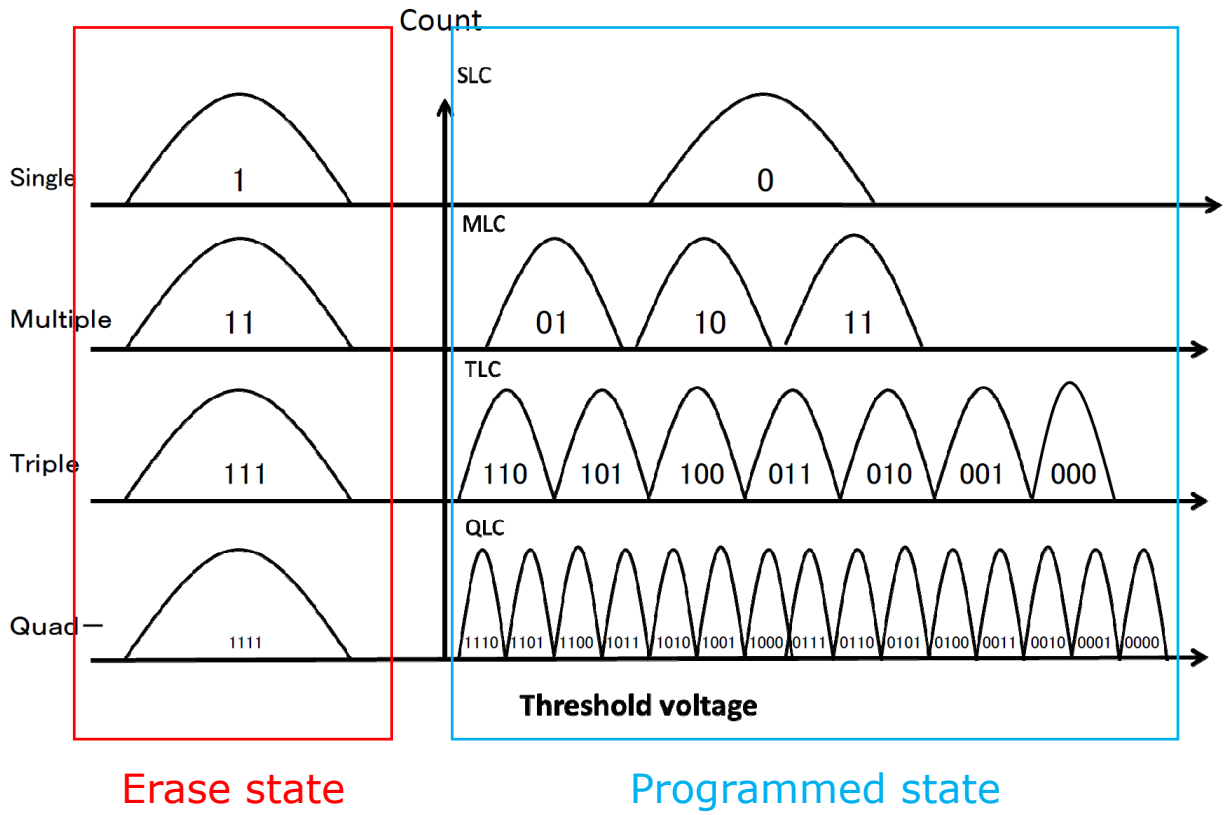
Rebuild Mapping Table

- We can store a mark when we programmed data into NAND Flash and use the mark to rebuild mapping table



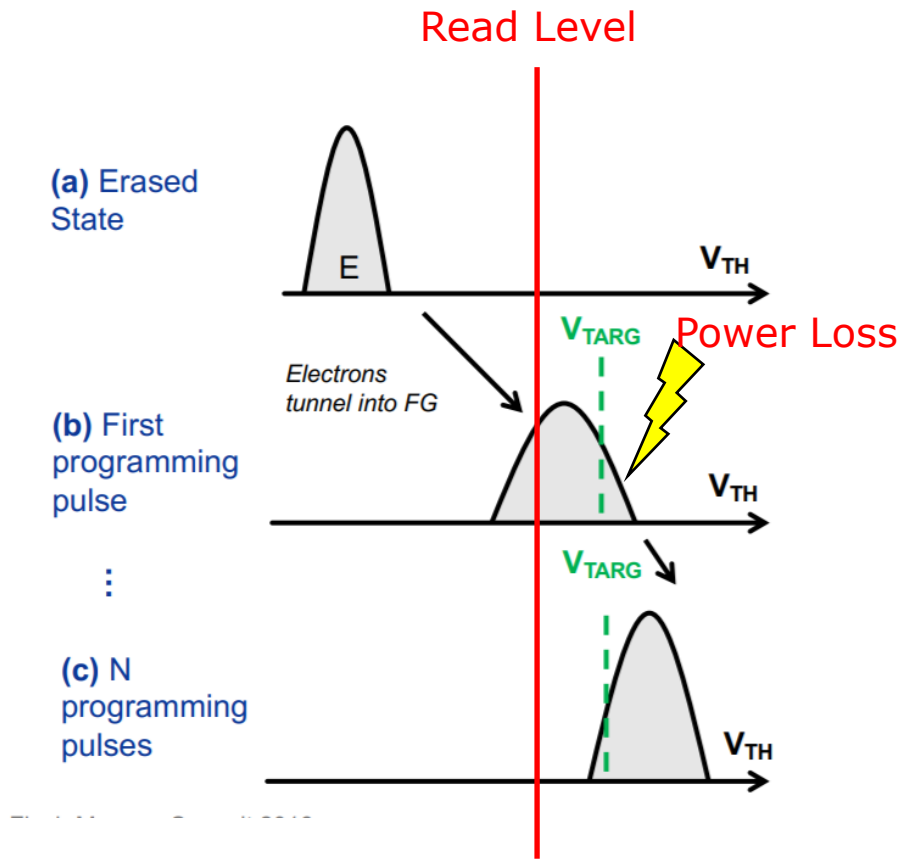
Power Loss

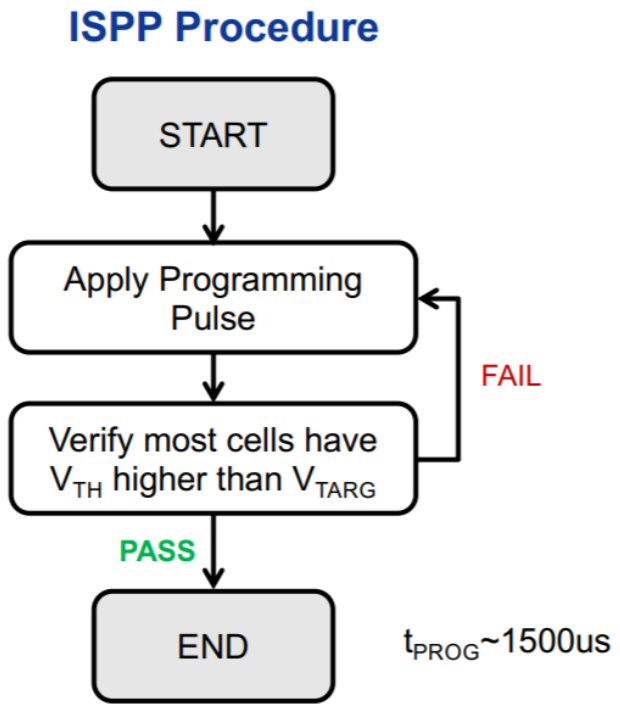
- When data is programmed, VT will shift from erase state (left) to programmed state (right).



Power Loss Detection

- What if sudden power loss happens before VT reaches programmed state?





Bad Block Management (BBM)

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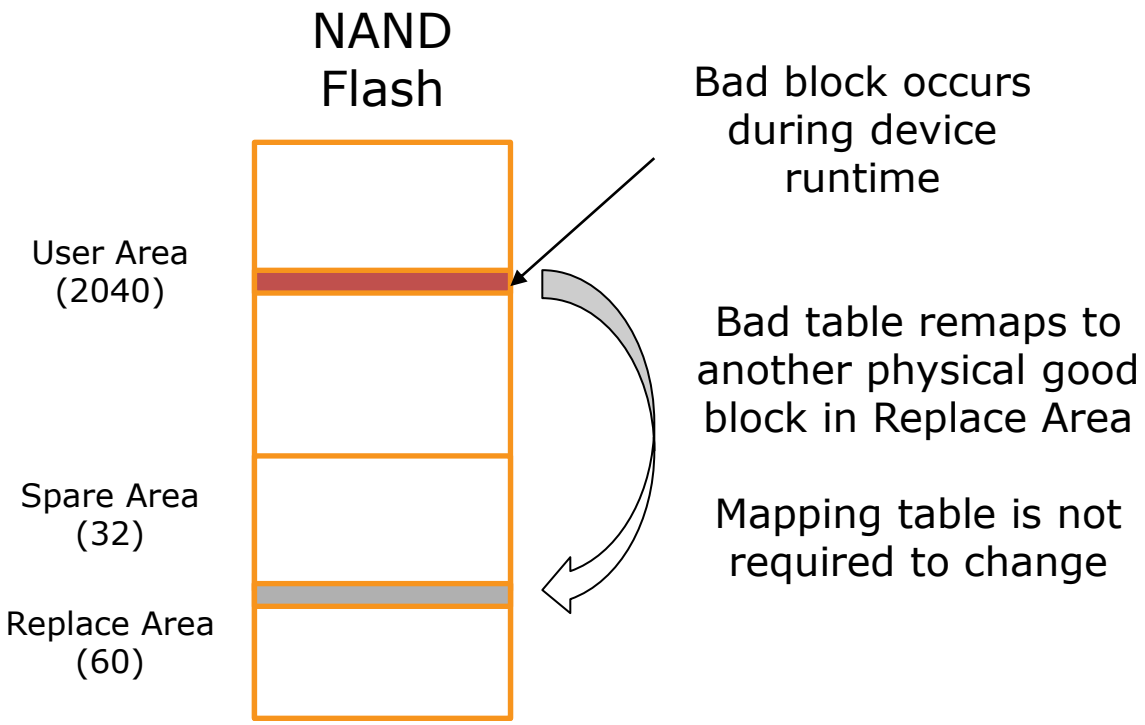
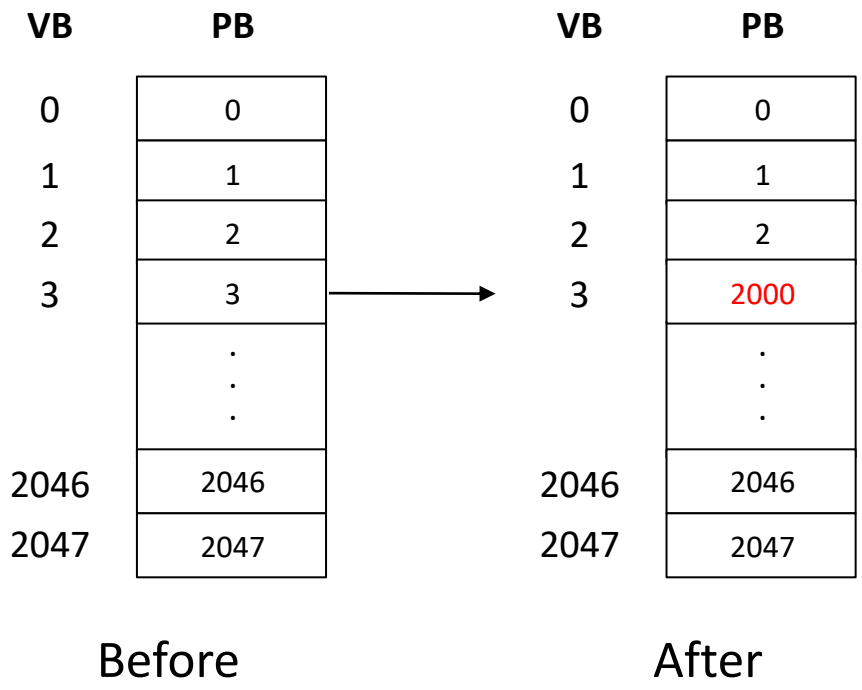
Background

- There are two types of bad blocks in NAND flash:
  - Initial bad blocks (due to production yield constraints)
  - Accumulated bad blocks (due to program/erase)

Solution

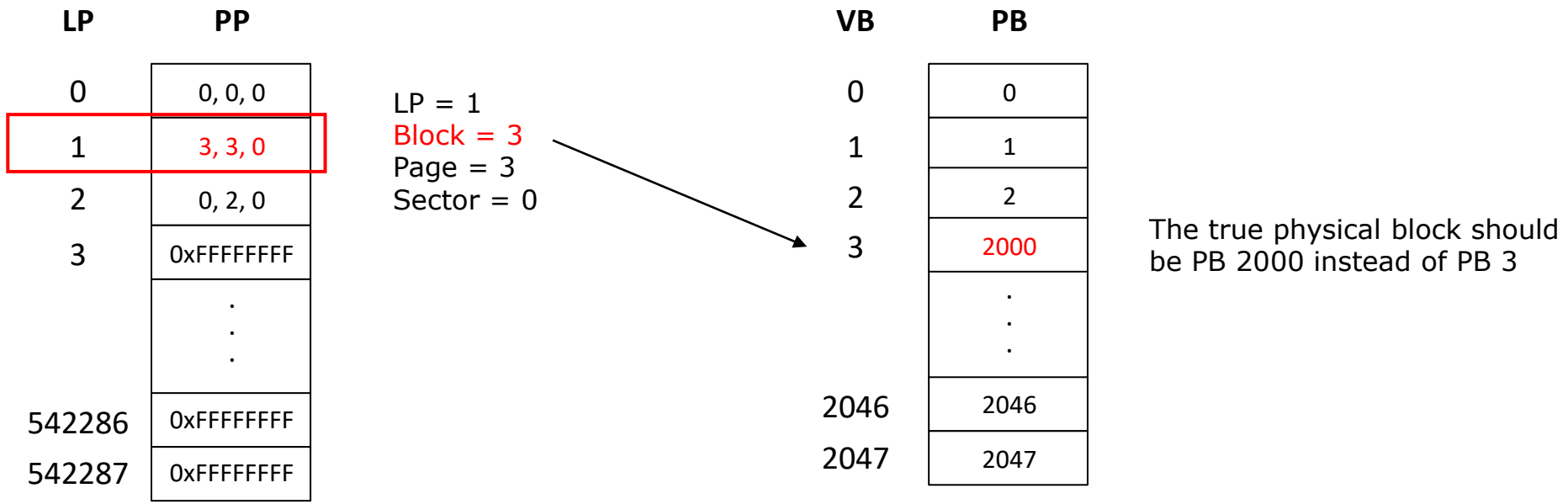
- Bad Block Management (BBM) is required to map out both initial bad blocks and bad blocks occurring during device operation
- We need to reserve some blocks for bad block replacement





Solution

- During L2P translation, after getting physical address from Mapping Table, we still need to check Bad Block Table for the true physical block address



Wear Leveling (WL)

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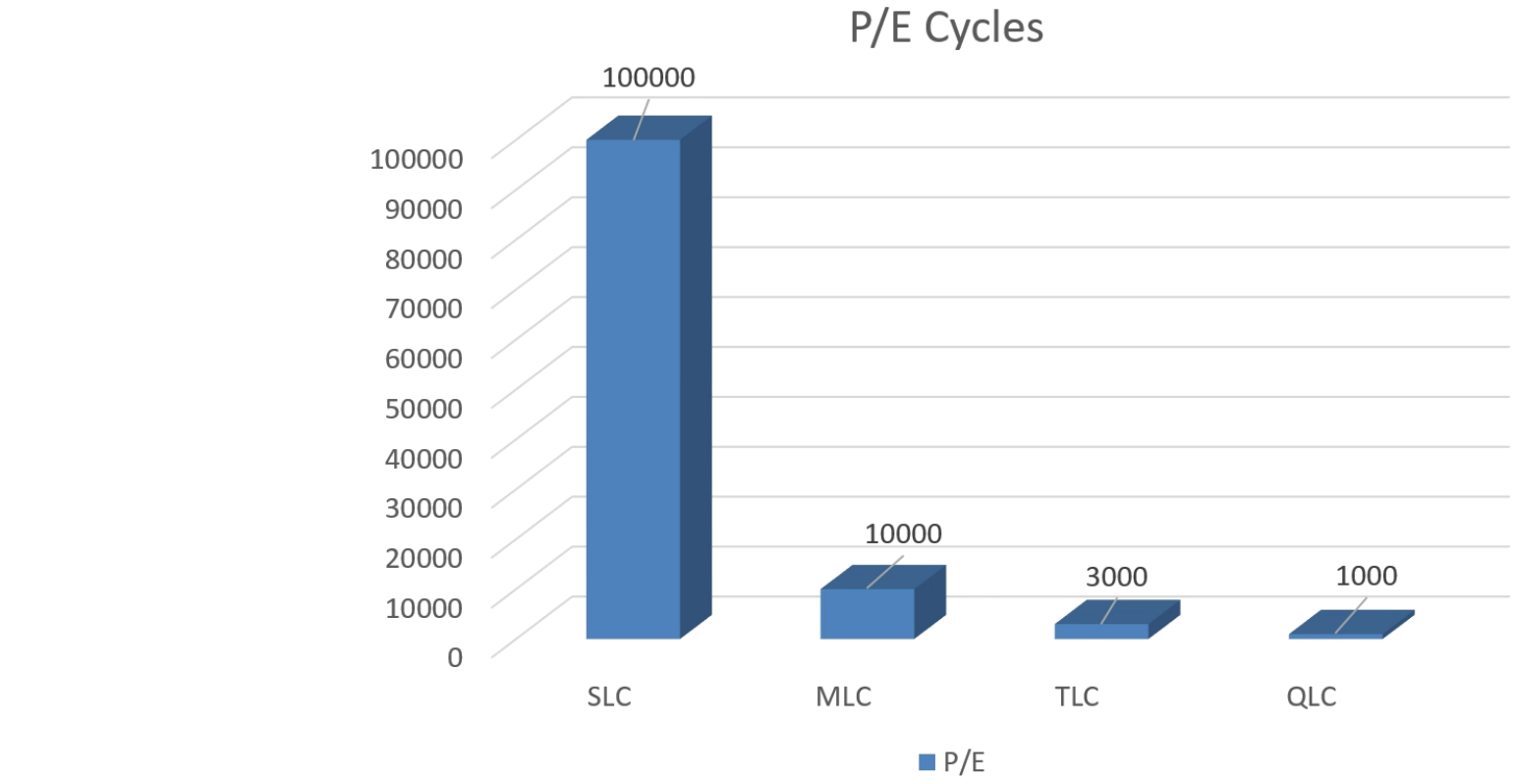
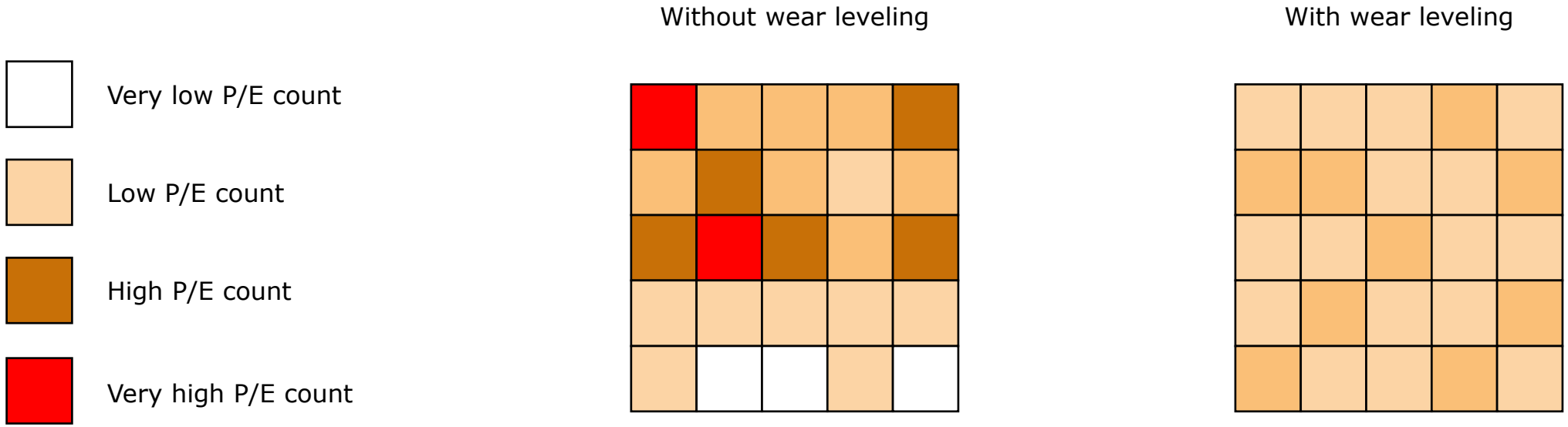
Background

- As we know, program/erase pulses will lead to degraded reliability of the underlying NAND flash cells
- When certain blocks has higher (or near to maximum) Program/Erase (P/E) cycles, they might produce more errors



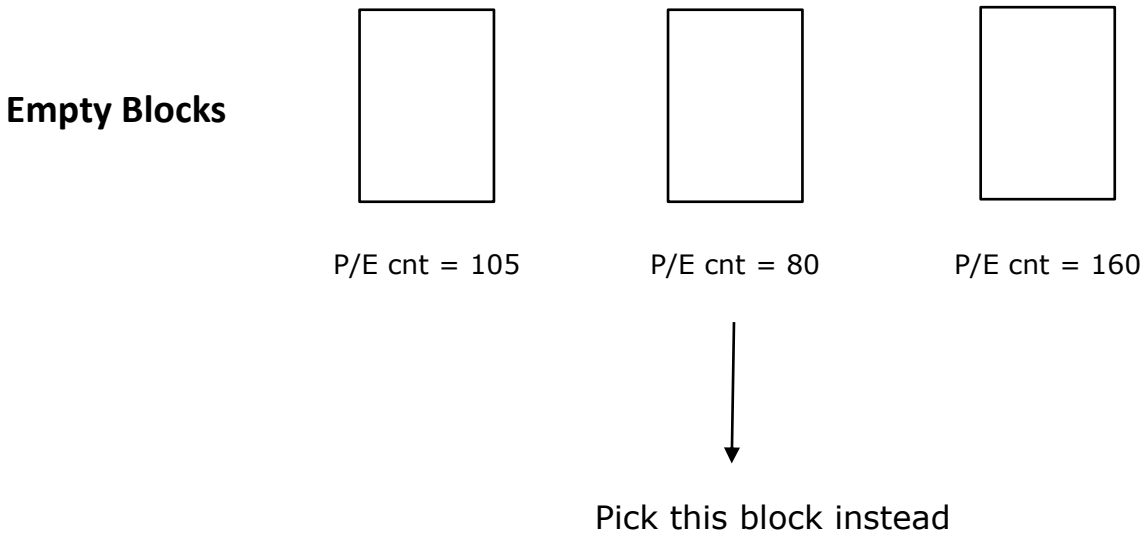
Background

- Without wear leveling, certain blocks will wear out faster than other blocks
- Remember the similar situation when we talked about low OP?



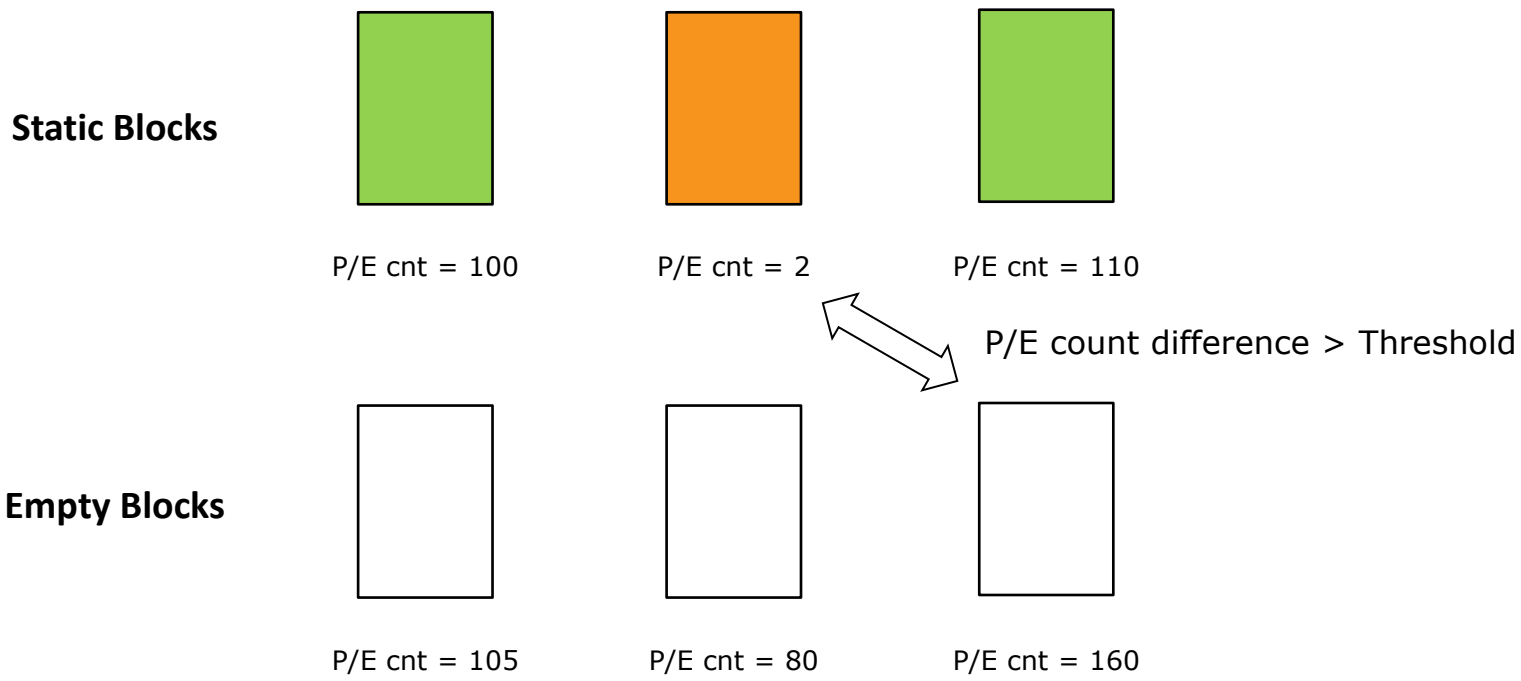
Solution

- Pick the empty block with least P/E count to use first



Solution

- Swap blocks if difference between max. P/E count block (in empty blocks) and min. P/E count block (in static blocks) exceed threshold



Summary

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Summary

- Read errors & disturbance
- Sudden power loss & rebuild
- Bad block management
- Wear leveling

Cold Facts

- Do you know that the reliability of your storage device is highly dependent on the NAND Flash technology (SLC, MLC, TLC or QLC) that it uses?
- Do you know that when you unplug your storage device when it is in the middle of read/write operation, your data might be corrupted?
- Do you know that when your storage device operates at different extreme temperature conditions, your data might be corrupted?

FTL

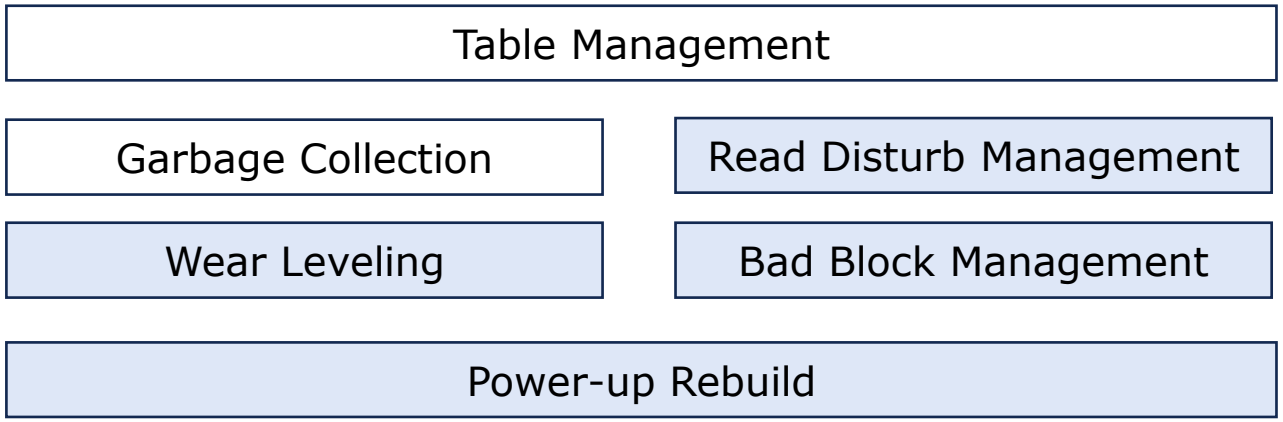
Table Management
Garbage Collection
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Wear Leveling
Bad Block Management
Power-up Rebuild

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THANK YOU!