Synthesis Verification by the SFG-Tracing: Methodology*

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Abstract.

In this presentation a novel and practical methodology which can be applied for formal correctness verification of digital (VLSI) designs is presented. This methodology aims at bridging the gap from transistor switch level circuits, as obtained from circuit extraction, up to high level specifications. The *SFG-Tracing* verification methodology inherits its power from the exploitation of the inherent algorithmic information the high level (signal flow graph level) specifications. Given the fact that the circuit designer provides the appropriate reference signals and mapping functions, the methodology has already successfully been experimented on the full formal verification of VLSI circuits of more than 32.000 transistors as extracted from the layout. This method is currently being used to automatically prove the correctness of the synthesis results from the CATHEDRAL-1 (bit-serial) and CATHEDRAL-2 (microcoded processor architectures) silicon compilers.

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