

***SFG-Tracing*: a Multi-Level Formal Verification Methodology.**

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The *SFG-Tracing* methodology for the multi-level verification of lower level implementations with respect to their higher level specifications is presented. This *SFG-Tracing* methodology is currently successfully being worked out for the automatic verification of the synthesis results of the CATHEDRAL silicon compilers. Here the feasibility has already been demonstrated by the verification of a 32,000 transistor modem chip implementation (containing 3 concurrently operating ALU's, microcode, multi-branch controller, circuits for testability, register files etc..) starting from the layout extracted SPICE transistor netlist up to the high level algorithmic specifications at the signal flow graph level as specified in the SILAGE language. The presented methodology is generally applicable (e.g. also for microprocessor designs).