Multi-Level Digital Design Verification by SFG-Tracing *

Luc Claesen [†] Eric Verlind, Marc Genoe, Frank Proesmans, Hugo De Man[†]

IMEC, Kapeldreef 75, B-3001 Leuven Belgium phone: +32-16-281203, email: claesen@imec.be

Abstract.

In this paper a novel methodology for the formal correctness verification of digital (VLSI) designs is presented. This methodology aims at bridging the gap from transistor switch level circuits, as obtained from circuit extraction, up to high level specifications. The SFG-Tracing verification methodology inherits its power from the exploitation of the inherent algorithmic information the high level (signal flow graph level) specifications. Given the fact that the circuit designer provides the appropriate reference signals and mapping functions, the methodology is intended to operate automatically on VLSI circuits of up to 100,000 transistors and more.

1 Introduction.

The possibilities offered by the steadily increasing complexities offered by the VLSI technology has resulted in the fact that more and more complex systems can be built on integrated circuits. The realization of complex systems has become *design limited* instead of technology limited. The challenge is indeed to design electronic systems *first time right*. This is required to avoid costly redesign, and delays in market introduction of new products. These economic reasons are the drive behind a lot of effort to check the correctness of designs with respect to their specifications.

Traditionally simulation (at multiple levels of design abstraction) is used, and is standard industrial practice, to verify the correctness of electronic designs before they are produced. It is however very well known that for even moderately sized circuits it is not possible to try out all possible input excitations in these simulations, due to the combinatorial explosion problem in the number of possible patterns. Therefore designers have to choose an appropriate subset of input stimuli for verification by simulations. This method however leaves open the possibilities for undiscovered design errors. This motivates the need for analytic verification techniques that are input pattern independent. The technique of *static timing verification* is an analytic technique that has currently gained industrial acceptance for the verification of the speed performance of circuits.

The analytic verification of the *behavioral correctness* of digital designs with respect to their specifications is however still in its infancy. It is mainly hindered by the problems of combinatorial explosion in handling the mathematical formulas describing the systems at hand.

Formal correctness verification techniques have been investigated already for a few decades in theoretical computer science. Although better insights have been gained in the mathematical modeling of computer programs, no full correctness proofs of practical computer programs can

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be done in a realistic way. Formal verification techniques derived from these developed in theoretical computer science have been applied in hardware designs and have been illustrated by the correctness proofs of small microprocessors using mechanical theorem proving methods [11, 12]. Even for these small sized applications, the correctness proofs require several months of (mechanical theorem proving) expert interaction for conducting the correctness proof. It is also not obvious how design specific theorems and proof strategies can be automatically generated from specifications or how they can be reused in new designs.

In the inaugural session of ECCTD'83, Dr. C.F. Kurth of Bell Labs USA gave a presentation on the impact of the evolution in circuit theory and technology on the design of communication systems. He presented circuit and systems theory as the basis for system analysis, CAD, VLSI, signal processing, DSP simulation and network synthesis. The technological evolution towards more economic solutions is going more and more digital. He pointed out that the mature circuits and systems theory is not appropriate for digital signal processing systems. He stressed that "the foundation of a new binary system theory will be a challenge for the next decades".

Nearly one decade later, we are at a point where a number of promising theories have evolved and are under further development that are part of such a useful "binary system theory". For the representation and manipulation of Boolean formulas, the ordered binary decision diagrams (OBDD's) [20] is currently the best known technique. It is currently used in the verification of combinatorial logic and in logic synthesis. Several additional techniques are still being proposed that improve the efficiencies that can be obtained. Analytic methods [14, 15, 18] have been developed that allow to extract symbolic equations from MOS switch level circuits, that accurately model bidirectional information flow, multiple strengths of nodes and transistors and 'X' behavior. For the verification of finite state machines (modeling the controlers in digital systems) promissing techniques have been worked out [2, 3].

The main breakthroughs in formal verification methods for *behavioral correctness* have been achieved by methods that take advantage by exploiting the circuit structure in the verification algorithms. This is the only way to avoid the problem of combinatorial explosion that results when trying to formulate the correctness problem in a general way (e.g. Boolean formulas) and have a general decision procedure trying to figure out the correctness.

Further along these lines of correctness verification we propose a method called SFG-Tracing that exploits the information available in the signal flow graph level specification that describes the algorithms to be implemented.

In this paper we present a new method for the automatic verification from the behavioral signal flow graph specification down to lower implementation levels. These can go down to the switch level if a suitable symbolic simulator is used. In line with the automatic verification algorithms, as much as possible the structure available in the problem at hand is being exploited. The first application target is in the verification of high level synthesis results as obtained by the CATHEDRAL silicon compilers [8, 9], but the methodology is generally applicable.

The algorithms are intended to operate with as little interaction from the user as possible. The underlying assumption is that the flow graph specification is synthesized while keeping track of mapping relationships of a set of well-chosen reference signals of the specifying flow graph and of the implementation. The global verification problem is reduced to a manageable size by partitioning the information in the global signal flow graph into acyclic subgraphs and providing correspondence (mapping) functions between the interface values (reference signals) in the partitioned graph and the signal values at specific cycle and clock phase times in the implementation. The correctness of each individual subgraph is proven by making use of a (switch-level) symbolic simulator that acts on the actual switch level models of transistor circuits.

To give an indication of the information explosion from high level (SFG) specifications down to the implementation, consider the modem pulse shaper and equalizer chip indicated in figure 1 and as designed by Vanhoof e.a. [10]. This system implements the filter flow graph indicated



Figure 1: Design & time abstraction levels from SFG (signal flow graph) down to transistor layout, for a receiver pulse shaper and equalizer, containing 3 ALU's of 14 bits as synthesized by CATHEDRAL-II

in the top of the figure and can be formally specified in the SILAGE language in 70 lines of text. The chip implementation as synthesized by CATHEDRAL-II [10] results in a microcoded architecture with 3 ALU's of 14 bits and consists of more than 31614 transistors. Near the figure is shown the time abstraction from sample periods at SFG level over micro-code instruction cycles, clock phases down to clock waveforms at the switch level. Notice that all the signals that appear in the SFG specification occur in some form during specific times at specific places in the transistor implementation of the chip. Operations in the SFG can however occur on the same hardware blocks such as ALU's at different instances of time. This relationship between algorithmic SFG signals and signals in space and time of the implementation forms the basis for the SFG Tracing verification methodology.

In this paper we give a short overview of the theoretical background of the SFG-Tracing methodology. For the relationship with existing formal verification methods and an overview of the inclusion of the methodology in a CAD environment, we refer to [5].

In the next section, we give an overview of the SFG-Tracing methodology.

2 SFG-Tracing Methodology.

The goal of the verification process is to verify the behavioral input-output correctness of the lower level implementation with respect to the high level signal flow graph specification. Of course it would be the most interesting to perform the verification from a level as high as possible to an implementation as detailed as possible. In this paper, we consider the SILAGE SFG level as the specification, and the transistor switch level as the representation. Higher levels of the implementation could also be considered (such as gate level or sRT or bRT level). The same techniques as indicated below would apply in each of these cases. The switch level implementation is however preferred, because it reflects the best the circuit implementation. Appropriate symbolic analysis techniques based on Bryant's method [14, 15] for the switch level have been developed and are supported in CAD tools [18, 16, 17].

2.1 Flow Graph Specification.

For the SFG-tracing, two aspects have to be considered. The first consists of the verification of the *initialization sequence*, and the second aspect consists of the verification of the *steady state behavior*. The initialization sequence is used to bring the implemented system into a known state. Starting from that known state, cycles and clock phases can be defined, which correspond to the SFG level sample periods. The initialization sequence consists of the sequence following for example the reset pulse. The symbolic simulator will have to be started from the initialization sequence in order to be able to bring the implemented system into a known state. The SFG specification also contains initialization information (initial values at SFG level registers). The verification will consist of two phases: the initialization and the steady state. Although similar techniques can be used for both phases, this paper will concentrate further on the verification of the steady state behavior.

2.2 Basic SILAGE Signal Flow Graph Semantics.

The basic SILAGE signal flow graph semantics are modeled by a graph $\mathcal{G}(V, E)$.

The set of vertices V of this signal flow graph \mathcal{G} are defined by vertices $v_i \in V$ corresponding to the primitive operations in SILAGE. Examples are: arithmetic operations (addition, subtraction, multiplication...), shift, logical operations and conditionals.

The set of edges is E is defined by edges $e_j \in E$, where each e_j corresponds to a signal in the SILAGE flow graph. In SILAGE, signals are defined as one-sided infinite streams, characterized by a specific sampling rate.

Two functions $Inputs: V \rightarrow E^*$ and $Outputs: V \rightarrow E^*$ can be defined: $Inputs(v_i) = \{e_k, e_{k+1}, ...e_m\}$ and $Outputs(v_j) = \{e_l, e_{l+1}, ...e_n\}$

which describe the inputs and outputs of operators in SILAGE. In SILAGE only one output is used per operator.

To each edge e_j corresponds a SILAGE *signal*, that is modeled as a stream. However at specific moments in the algorithm time t_{sfg} , individual element values of the stream can be considered $e_j(t_{sfg})$. The signals can be words representing numeric binary values of a specific word length w_{e_j} . The signal consisting of a binary word can be represented as $e_j[1..w_{e_j}]$. It is assumed that individual bits in signals representing binary values are ordered from most significant bit (MSB) (index 1) to the least significant bit (LSB) (index w_{e_j}). The k'th individual bit of the signal e_j is represented as $e_j[k]$.

2.3 Reference signals and Mapping functions.

In SFG-Tracing we make the following assumptions:

1. There exist a number n_{ref} of reference signals $e_r \in RefSignals(\mathcal{G}(V, E))$ corresponding to edges in the SFG algorithm specification and signals at specific (cycle and clock) times in the implementation. The specification SFG is implemented in hardware maintaining the same behavioral relationships for these reference signals.

For all reference signals $e_r \in RefSignals(\mathcal{G}(V, E))$ the signals e_r^s in the specification and e_r^i in the implementation can be defined:

• The reference signals in the SFG specification $e_r^s(t_s)$ have the following semantics in terms of Boolean bit words:

$$e_r{}^s[k_s](t_s) \in \mathcal{B} \tag{1}$$

for all bits $k_s \in \{1..w_s\}$ in the SFG signal word and for a specific sample time t_s . B is the set of Booleans. Often at the SFG level, the individual bits in signal words are not considered.

The reference signals in the implementation are characterized by:

$$e_r{}^{i}[k_i](t_{ik_i}) \in \mathcal{B}$$
⁽²⁾

for individual bits with index $k_i \in \{1..w_i\}$ at specific implementation times t_{ik_i} . The index k_i of t_{ik_i} indicates that each bit of a reference signal has to be considered at a specific cycle and clock phase individually. This is for example already necessary in bit-serial implementations of SFG specifications.

2. There exist a set of mapping functions \mathcal{F} that describe the behavioral correspondence in space and time of reference signals in the SFG algorithm specification with respect to the lower level implementation at the specific implementation times.

$$\mathcal{F}: Switch_signal_semantics \to SFG_signal_semantics$$
(3)

or:



Figure 2: Illustration of the concepts of *reference signals* and *mapping functions* that relate signals in the SFG specification to signals in lower level implementations. (Here down to the switch level).

$$\mathcal{F}: \mathcal{B}^{w_i} \to \mathcal{B}^{w_s} \tag{4}$$

where \mathcal{B} is the set of Boolean values.

The function \mathcal{F} is defined as:

$$e_r^{s}(t_s) = \mathcal{F}(e_r^{i}[1](t_{i1})...e_r^{i}[w_i](t_{iw_i}))$$
(5)

This is a vector assignment over the individual bits of the reference signal in the SFG.

- 3. All edges and vertices in $\mathcal{G}(V, E)$ are reachable via directed paths starting at the edges corresponding to reference signals.
- 4. The reference signal partitions the graph $\mathcal{G}(V, E)$ such that the subgraphs are acyclic.

The most essential form of *reference signals* would be the input and the output to the algorithm to be implemented in hardware. The verification effort and complexity can be reduced if more reference signals are available.

The concept of reference signals and mapping functions is illustrated in figure 2.

For the reference signals it is required that mapping relations are available, which state the relationship between reference signals in the specification and in the implementation. This could be in the form of a certain word at a specific sample time in the SFG level begin implemented in terms of bits in specific registers (at specific time phases) at the lower level implementation. Most of the relationships will be simple correspondences of the logic values in specification and implementation. Other relationships could include a specific logic function to convert the logic representation in the specification into the logic representation in the implementation or vice versa. The simplest form of this are signals in the specification that are identical or inverted in the implementation. However, more complex relationships can be envisioned: e.g. an integer word at the SFG level represented in the implementation in carry save technique.

The third condition is required so that the SFG Tracing algorithm can use a directed graph traversal algorithm to reach all of the parts in the specification SFG in order to do the comparison.

2.4 Signal Flow Graph partitioning.

The choice of appropriate reference signals and mapping functions allows that SFG graph $\mathcal{G}(V, E)$ is partitioned into a signal flow graph PSFG (Partitioned Signal Flow Graph) consisting of a set of disjoint and acyclic subgraphs $\mathcal{G}_p(V_p, E_p)$. Each subgraph $\mathcal{G}_p(V_p, E_p)$ consists of a cutset of vertices of $\mathcal{G}(V, E)$ where the edges between vertices in the cutset and vertices out of the cutset correspond to the reference signals, related to that subgraph.

2.5 Description of the SFG-Tracing method.

The reference signals allow a subdivision of the global SFG in a number of subgraphs in the PSFG. For each subgraph in the PSFG a verification of the implication of the specification by the implementation is verified by performing a symbolic simulation of the implementation.

```
SFG_Tracing()
{
    read_reference_signals_and_mapping_functions();
    init_symbolic_simulation();
    PSFG = Partition_SFG();
    for each subgraph in the PSFG
    {
        for impl_time = start_time to end_time;
        {
            for impl_time = start_time to end_time;
            {
                symb_initialize_impl_signal(impl_time);
                symbolic_simulate_step(impl_time);
            }
        symb_compare_signals();
    }
}
```

In read_reference_signals_and_mapping_functions(); the reference signals and the mapping functions are read. Making use of this information the partitioning of the signal flow graph is performed in Partition_SFG. Hereafter for each subgraph the verification is done by a symbolic simulation. Since reference signals in the implementation can occur in different cycles and clock phases, (within a global SFG clock period of the system) the values of implementation signals have to be initialized in the symbolic simulation at the appropriate implementation times. Therefore the symbolic simulation has to be done from start_time to end_time, such that all the signals that are input to the PSFG subgraph can be initialized and that after that, all signals at the output of the PSFG subgraph can be evaluated in the appropriate cycle time and clock phases.

In the symbolic simulation, the reference signals and the signals dependent on them will be evaluated symbolically. External signals that are always recurring during each global SFG time period will have specific values. This is the case for external clock signals, that will be used for the specific values in the respective phases. Other signals such as reset signals and signals to put the circuit in test mode, will be set to the specific constant values. Doing such a symbolic simulation will result in specific (Boolean 1,0) signals for the control circuits, and symbolic signals for the other circuitry. Most of the time 'x' signals will be used in the symbolic simulation. Only for those signals implementing the operations of the subgraph of the PSFG at hand, symbolic values will be computed. The controller takes care of the sequencing in time of the hardware operations that have to be performed on the same hardware operator (e.g. the same ALU). By doing symbolic simulation, the effect of the sequencing by the controller is removed, and the hardware operators can be seen as unfolded for the specific operations that they have to perform.

By this symbolic simulation, the micro-code controller will normally operate with instantiated signal values ('1', '0', 'x') instead of symbolic values in the execution of cycles and clock phases. These instantiated signal values can directly be used (and reduced) in the symbolic simulations. By this fact of unfolding (or unrolling) the algorithm again to its maximally parallel representation the effect of the controller, and its specific encodings can be 'simulated away'.

After the symbolic simulation, symbolic expressions are obtained for the output signals corresponding to the subgraph under consideration. Notice that these symbolic output signals have to be taken at the appropriate cycle and clock phase times as defined by the reference signals. As already explained these output signals correspond to the maximally parallel representation as in the SFG specification, and the correctness has to be verified by comparison.

From the semantic definitions of the primitive operations in the specifying SFG, the mapping functions for the reference signals (that form the interface for the subgraph at hand), and the results of the symbolic simulation a comparison is done in symb_compare_signals.

From the semantics of the primitive operators in the subgraph of the PSFG under consideration, the input-output behavior at the SFG level for the subgraph can be derived. This is characterized by the function:

$$S_{sfg}: \mathcal{B}^* \to \mathcal{B}^* \tag{6}$$

This function provides the behavioral relationship as extracted from the SFG semantics between reference signals at the input $e_{r_{in}}^{s}$ and at the output $e_{r_{out}}^{s}$ of the subgraph under consideration:

$$e_{r_{out}}{}^{s} = \mathcal{S}_{sfg}(e_{r_{in}}{}^{s}) \tag{7}$$

In the same way the input-output behavior function as derived by the symbolic simulation of the implementation can be defined:

$$\mathcal{S}_{impl}: \mathcal{B}^* \to \mathcal{B}^* \tag{8}$$

This function provides the relationship as obtained by the symbolic simulation between reference signals at the input $e_{r_{in}}$ and at the output $e_{r_{out}}$ of the subgraph under consideration:

$$e_{r_{out}}^{i} = \mathcal{S}_{impl}(e_{r_{in}}^{i}) \tag{9}$$

The mapping functions for the reference signals at the inputs and outputs of the subgraph under consideration provide the following relationships:

$$e_{r_{out}}^{s} = \mathcal{F}_{r_{out}}(e_{r_{out}}^{i}) \tag{10}$$

and:

$$e_{r_{in}}^{s} = \mathcal{F}_{r_{in}}(e_{r_{in}}^{i}) \tag{11}$$

From the above relationships, the subgraph behavioral functions and the mapping functions, the following condition for the correct behavioral verification of the subgraph under consideration can be derived:

$$\mathcal{S}_{sfg}(\mathcal{F}_{r_{in}}(e_{r_{in}})) = \mathcal{F}_{r_{out}}(\mathcal{S}_{impl}(e_{r_{in}}))$$
(12)

The verification will normally be done by tautology checking, based on efficient methods such as OBBD's [20]. In this comparison, one can however also make use of the information available from the signal flow graph, such as the fact that at the SFG level signals are representing bitwords. Optimized verification algorithms and vector-based reduction rules such as presented by Eveking [23] and Simonis [22] can be used to improve the cpu-time efficiency of the verification.

3 Current Results and Future Work.

The manual application of the SFG-Tracing digital design verification methodology by means of an illustrative example of a BCD-recognizer is presented in [6]. The SFG-Tracing methodology is currently being worked out for proving the correctness of the synthesis results in CATHEDRAL-I [8] and CATHEDRAL-II [9]. The feasibility of the full formal verification of both of these silicon compilers has been demonstrated by representative application examples. In [24] a number of full formal verifications of circuits starting from their layout-extracted transistor networks are described. This includes the modem chip in figure 1 which consists of 31,614 transistors. For this the COSMOS compiled code switch level simulator [14, 15] has been used. Future research work is concentrating on the automatic generation of the reference signals and mapping functions from the high level synthesis. Is very important to be able to start from the layout extracted transistor circuits, because they capture the ultimate CAD information before mask making. Therefore current research concentrates onsymbolic simulation capable of analyzing circuits of the order of magnitude of 1,000,000 transistors.

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