SLOCOP : A TIMING VERIFICATION TOOL FOR SYNCHRONOUS CMOS LOGIC

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Abstract

In this paper, a new, accurate method for timing characterisation of synchronous CMOS circuits, described at transistor level, is presented. It is implemented in a computer program SLOCOP. SLOCOP first performs a knowledge based partitioning of the circuit into registers and combinational subcircuits, verifies high level timing rules (clock phasing) and finally detects longest signal propagation paths, with an accuracy comparable to device level simulation. Besides the delays of the critical paths, SLOCOP generates test patterns that activate these paths. The test pattern generation algorithm eliminates false paths and allows the designer to check the delay by an overall simulation. For delay calculation, local simulation is done with accurate SPICE-like transistor models. Critical paths are graphically displayed using hierarchical backannotation to a schematic. Deviations between estimated and real (simulated) delays are typically within 5% for static CMOS circuits. Pass transistor logic may give larger errors which remain however within 10%.

Introduction

Until now, timing characterisation of combinational logic is mostly done by simulation of the circuit at device level. This consumes large amounts of CPU time and is unreliable when the designers have to indicate critical paths themselves.

To address this problem, several computer programs have been developed for timing analysis of MOS circuits (1,2). These programs do not require the user to provide input patterns but pinpoint critical paths. They are mostly based on the assumption that the circuit can be split up into smaller subnetworks. To calculate the delay of those subnetworks, approximative methods (mostly based on RC modeling) are used in these approaches. The RC model is responsible for potentially large errors in the global delay estimation. It also restricts the class of circuits that can be handled. In contrast, SLOCOP uses local circuit simulation for delay calculation. This method is more time consuming than RC calculations, but it is very reliable, much more accurate, and applicable to any type of subnetwork that can be described in its knowledge base.

For the global analysis, graph algorithms are used. Exhaustive path search is not possible due to the large number of paths. In CRYSTAL (1), an algorithm is used that calculates the slowest settling time at each node in the circuit. SLOCOP however uses a critical path algorithm which provides the longest signal propagation paths from inputs to outputs, because this information is essential in the timing optimisation phase of the design.

Characteristics of the program and algorithmic aspects.

SLOCOP performs the following sequence of algorithms :

- In a preprocessing step, the transistor circuit is checked for consistency with topological design rules. This is done by partitioning the network into the basic subnetworks that are possible in a given design style. The description of the topology of those subnetworks (static CMOS gates, pass transistor trees with or without bleeder transistors,...) resides in a knowledge base. This knowledge base is written in a LISP-like language called LEXTOC (8). Therefore, in contrast to e.g. CRYSTAL, it allows to easily extend the program with new types of subnetworks, and makes it applicable to any definable class of digital MOS circuits (Fig. 4).

- Logic reduction algorithms transform each subnetwork into an equivalent network of AND, OR, NOT and MUX operators (Fig. 1a)(3,4). The last operator is necessary to model subnetworks which can have a high impedance output state.

- Circuits are assumed to be synchronous and clocked with a 2 phase not overlapping clocking scheme. Latches are automatically detected in the equivalent logic network and a partitioning in combinational blocks is done. Violations of clocking rules are reported (e.g. loops without latches on alternating clock phases).

- Timing analysis then consists of finding the longest signal paths from latch outputs to latch outputs clocked on the opposite phase. The SLOCOP method consists of accurate characterisation of the individual subnetworks by local circuit simulation. The set of input patterns that is needed to fully characterise the subnetwork for all possible signal propagation modes is automatically derived from its logic function. This set consists of a number of dynamic input vectors.
A dynamic input vector (DIV) contains elements that can have one of the four values 0, 1, U, D. U(p) represents a transition from 0 to 1, D(own) from 1 to 0. We restrict ourselves to DIV's in which only one element has a transition value. This makes it practically possible to find all DIV's that cause the output to make a transition (Fig. 1b).

- A signal propagation graph (SPG) is set up. The vertices in the SPG are inputs and outputs of subnetworks described in the knowledge base. Each edge corresponds to one DIV. The tail of the edge is the input that makes a transition, the head of the edge is the subnetwork output (Fig. 1c).

- A delay value is associated to each edge in the graph. Delay calculation is done by automatic local simulation of the subnetwork at device level. For this purpose, use is made of SIMMY, a PASCAL simulation module defined as an abstract data type (4). Input of the module is the transistor network and the DIV corresponding to the edge. To estimate the slope of the input transition, the subnetworks are leveled first. Local simulation is done in topological order. The average of the slope of the output waveforms of the driving subcircuit

(which is always simulated first) is taken as the slope of the input waveform. Output of SIMMY is the response waveform at the subnetwork output, with SPICE accuracy. Delay and slope are calculated by interpolation in this piecewise linear waveform. If the delays are measured at the same threshold voltage for each subnetwork, the path delay is the sum of the individual delays of the edges (Fig. 2).

- An algorithm is implemented that finds the N longest paths in the SPG. The time complexity is O(N**2), but linear with the number of edges and vertices in the graph, which is in turn proportional to the size of the circuit. The results are sequences of edges that form the longest, second longest,... signal paths. These paths are graphically displayed by highlighting the nodes that make a transition on the schematic. As SLOCOP is capable of handling circuits of up to a few thousand devices, hierarchical backannotation is implemented. This means that several cells in the hierarchy are displayed simultaneously and nets are highlighted at each level (Fig. 3).

- Each of the path edges corresponds to a local dynamic input vector for a subnetwork. This means that for all subnetwork inputs that do not make a transition, assumptions are made for the logical states of these nodes. Test pattern generation techniques are applied to derive a dynamic input vector at the inputs of the combinational blocks (primary inputs or latch outputs), which guarantees that those logical states are set. The global DIV has an U(p) or D(own) entry for one of the inputs, and 1 or 0 entries for all other inputs.

The algorithm may in some cases find that no global DIV is possible, because of conflicting assumptions imposed by the local DIV's for the subnetworks. In contrast to existing timing verifiers, 'false' paths (signal paths that can never be excited) are automatically excluded in this way. The test pattern allows to check path delays with global simulation.

SLOCOP performance and error analysis

Two approximations have to be made when the signal propagation delay through a subnetwork is extracted by simulation.

1. The load of the subnetwork, formed by the subnetworks that are driven by it, is modeled by an equivalent capacitor. The algorithm to derive the input capacitance of a subnetwork from its topology depends on the type of the subnetwork (static gate, pass transistor tree...). It will be discussed in the presentation.
2. The waveform used in SLOCOP for the input transition is an average of the linearised output waveforms obtained for the driving subnetwork. This may give errors in two ways :
   - The slope is not exact.
   - Replacing the real waveform by a ramp waveform has an effect on the output waveform and therefore on the delay measured. This effect is more significant when the waveform is applied to a pass transistor network than to a gate.

The run time of the program in its current version is almost exclusively spent in the subnetwork simulator. Subnetwork partitioning, logic reduction, longest path search and test pattern generation together take only a few percent of the total run time. It is obvious that a tradeoff between accuracy and speed can be obtained by using simulation techniques such as in ELOGIC or CINNAMON (6, 7, 9). This is a direction for further work on SLOCOP.

Results

A variety of circuits has been analysed with SLOCOP. An example is a 10 bit counter in static CMOS. Fig. 3 shows the multiwindow hierarchical schematic on which the critical path is highlightened by the program. The deviation between the path delay estimated by SLOCOP and the delay measured with an overall simulation is 4.2%. The circuit contains 240 transistors and was analysed in 157 seconds on a VAX 8600 computer.

The critical path is the carry propagation through the half adder cells. Test pattern generation gives us the state of the counter at which the maximal delay occurs.

Conclusions

A method for timing analysis is presented. It is applicable to a very wide class of MOS circuits, the only requirement being that the circuit can split up into relatively small unilateral subcircuits. The topology of the possible subcircuit types for a given design style must be defined only once in a special purpose language. The way the results are graphically presented to the user and the reliability of the estimated delays make it a valuable tool in the design and timing optimisation phase of large circuits.

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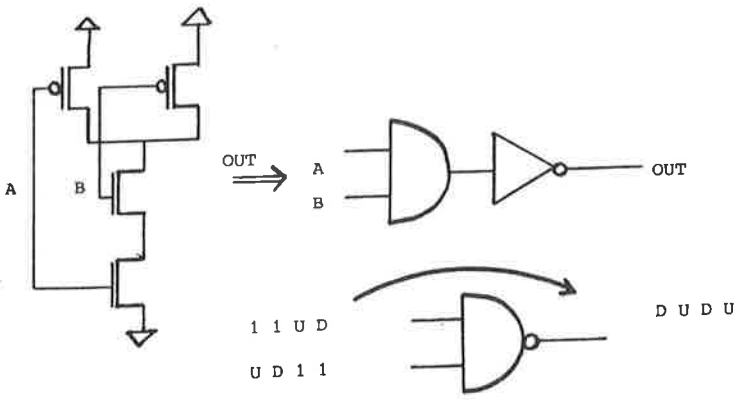

Fig. 1.a. Logic reduction

Fig. 1.b. Dynamic input vectors for a NAND gate.

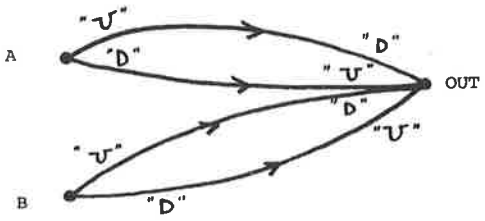

Fig. 1.c. Corresponding edges in the SPG graph. ("D" = transition 1 -> 0, "U" = transition 0 -> 1).

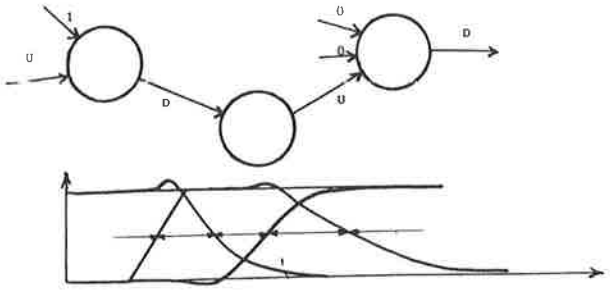

Fig. 2. Path delay = sum of subnetworks delays.

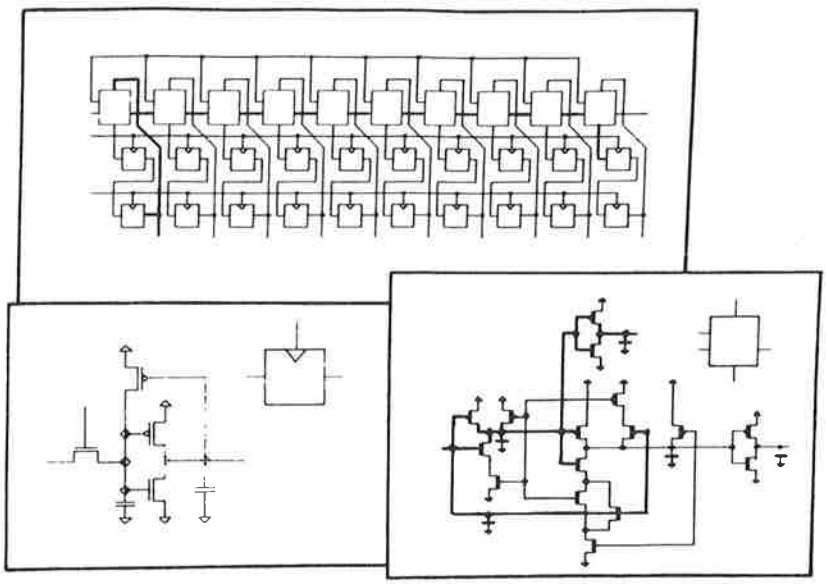

Fig. 3 Critical path in a counter circuit as highlighted by SLOCOP. The path starts at a latch output and stops at a latch input. Backannotation is hierarchical.

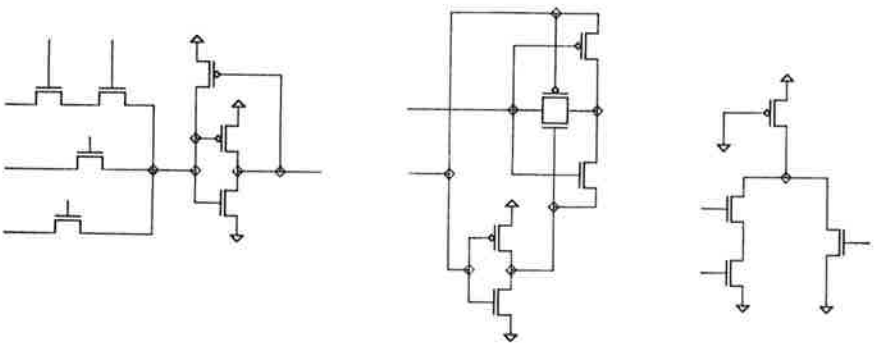

Fig. 4. Examples of subnetwork types described in the knowledge base of SLOCOP.

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