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DIANA.SC – a versatile top-down analysis tool for switched-capacitor circuits

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In this paper a general and designer-oriented top-down switched capacitor analysis tool, DIANA.SC is presented. The top-down feature of DIANA.SC allows for the analysis at a top level with ideal SC-circuits, at an intermediate level with SC-circuits containing resistors and op-amp poles and at a low level containing MOS-transistors and non-linear capacitors. The basic features and analysis modes at each of the levels are explained and illustrated. Several practical examples indicate the analysis levels and operation modes.

1. Introduction

In recent years switched capacitor circuits (SC-circuits) have become very popular[1,2] as an economical and very efficient means for realising on-chip filters. Together with this evolution a number of synthesis methods for SC-circuits have been proposed. A big problem was that no computer analysis tools were available. These analysis tools are needed to evaluate the performance of a design, to compare different design methods, to select component values and to analyse the different non-ideal effects. This can allow one to verify designs and avoid costly processing re-runs in hardware debugging. In answer to this need a number of analysis methods have been published[3-5, 20-27] of which most have been implemented by computer programs.

Although many programs for the analysis of SC-circuits have been proposed, most of them are applicable only to specific cases (e.g. limited to two phases, frequency domain analysis only, no continuous input-output couplings). One of the first more general and designer-oriented approaches in this computer analysis has been realised by the DIANA-program.[3] In ref. [3] DIANA was presented as a general and efficient simulation tool for SC-circuits, A/D- and D/A- converters. It allowed for DC, time-domain and frequency-domain response calculations for arbitrary clock cycles and many types of input. In the time domain circuit analysis mode, the program allows for resistors and non-linear elements. Even a mixed mode analysis of a switched capacitor circuit together with control logic is possible. Various examples of these modes are shown in ref. [3].

Since the publication of ref. [3], considerable enhancements have been made in the program and the purpose of this paper is to show how DIANA has been extended and optimised for the full top-down analysis of SC-circuits including most effects possible. Then the new CAD aspects of DIANA available for the user are illustrated with practical examples.

The more theoretical basis of this implementation is the subject of many other publications[3...12] and some others are in preparation.

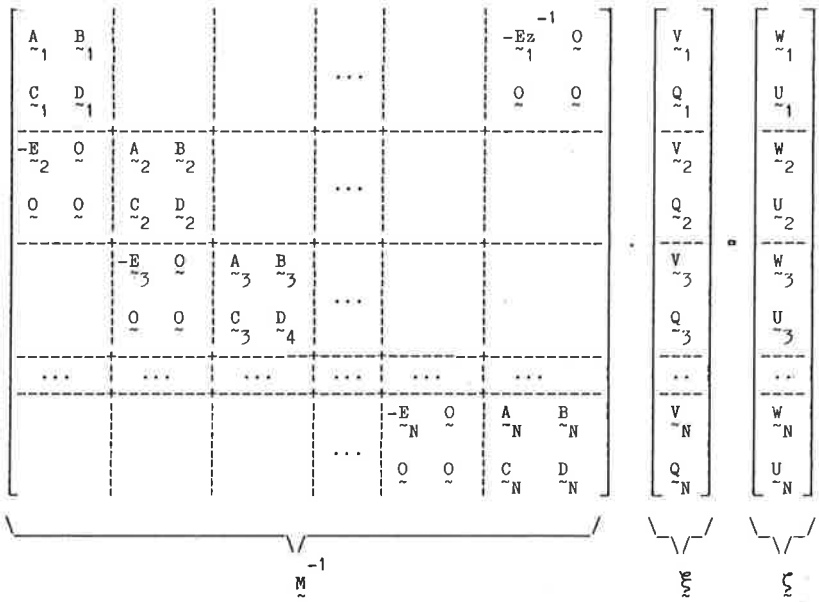
2. Evolution of the DIANA-program for the analysis of SC-circuits

The early frequency domain analysis method of DIANA[3] was based on a time-domain analysis for SC-circuits, which could easily be adapted from existing circuit analysis techniques.

Frequency domain analysis was performed by first calculating all the necessary impulse responses, doing Fast Fourier Transforms (FFTs) and combining the different results. This frequency domain analysis resulted in rather long CPU times.

In contrast, the algorithms in the current DIANA program are based on a general theory, which is useful for a computer aided analysis of SC-circuits in the time-, direct frequency- and z-domain and have been presented in ref. [4]. By combining the modified nodal analysis (MNA) and z-transform techniques, arbitrary SC-circuits can be described without topological restrictions.

According to ref. [4] this results for an N-timeslot SC-circuit in a matrix equation:



$$\ldots (1)$$

which relates the input z-transform of voltage U_i and charge sources W_i to the output z-transforms of node voltages V_i and charges in selected branches Q_i.

The transmission function from a signal with frequency Ω at the input to the component at frequency ω at the output has been shown[4] to be:

$$X(\omega, \Omega) = \sum_{k=1}^{N} \left\{ \nu_k(\omega) \sum_{l=1}^{N} H_{kl}(e^{j\Omega T}) \exp[j(\Omega t_{l+1} - \omega t t_k + 1)] + [\nu_k(\omega - \Omega) - \nu_k(\omega)] \exp[j(\Omega - \omega) t_{k+1}] H_{kk}(\infty) \right\} \quad \ldots (2)$$

$$\nu_k(\rho) = 2\{\sin[\rho(t_{k+1} - t_k)/2] \exp[j\rho(t_{k+1} - t_k)/2]\} / T\rho \quad \ldots (3)$$

Here the matrices H_{ij} are the submatrices of the inverse matrix M^{-1} eqn. (1) and indicate the transfer function matrix of the voltage sources U_j in timeslot j to the node voltage responses V_i in timeslot i. t_{i+1} is the time at the end of timeslot i. T is the clock period of all the clocks in the circuit. The first term on the right-hand side of eqn. (2) determines the transfer function of a piecewise constant input signal. The second term handles the remaining input signal which causes the continuous input-output coupling. The expression eqn. (3) takes care

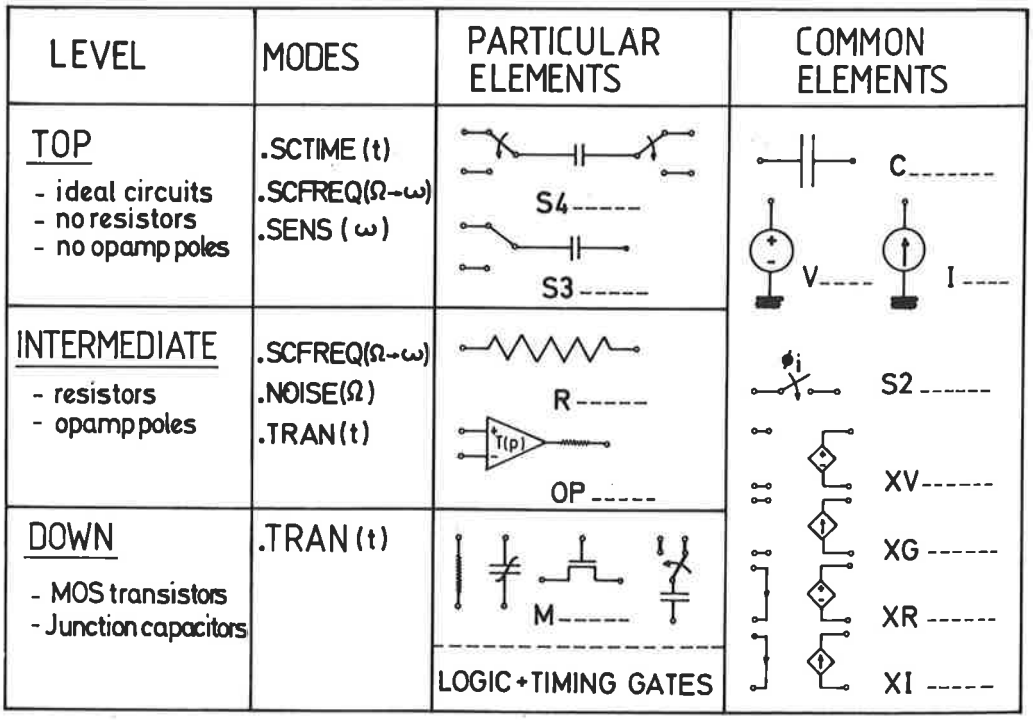


Fig. 1 Simulation levels with the possible analysis modes and elements in DIANA.SC.

of the sin(x)/x effect due to the sample and hold.

The set-up of the submatrices A_i, B_i, C_i, D_i and E_i in eqn. (1) can be formalised by using appropriate element stamps. In order to analyse the frequency response, the large matrix equations in eqn. (1) must be solved for every frequency point.

By this method multi-timeslot SC-circuits with arbitrary periodic clock cycles and with continuous input-output coupling can be handled.

For sensitivity- and noise analysis the above introduced analysis method[4] needs p+1 analyses in the case of a sensitivity analysis with respect to p parameters and needs p analyses in the case of a noise analysis of p noise sources. In ref. [5] the introduction of the adjoint network for SC-circuits allows for a more efficient sensitivity- and noise analysis. Only a maximum of two analyses needs to be done: one for the direct and one for the adjoint network. The matrix of the adjoint network can be obtained from the transpose matrix of the direct networks.[5]

The analysis method presented in refs. [4] and [5] could be optimised for a computer implementation by making appropriate combinations of terms in the expressions.[7] The theory in refs. [4] and [5] often results in a large matrix eqn. (1) which is sparse and the size of which is proportional to the size of the network and the number of phases (N). A matrix compaction algorithm has been worked out which reduces the matrix size to a number which is usually smaller than the sum of the number of inputs and outputs and the order of the filter.[7,8] Because of the special band structure of this matrix the factorisation part of the LU-decomposition can be done stepwise per timeslot part in eqn. (1) and needs to be done only once for all timeslots except for the last. To fully exploit the sparsity of the matrix a specially tailored (using a row index, column pointer scheme) sparse matrix storage system has been set up for matrix storage.

All the above mentioned analysis methods are valid if there are no transient effects e.g. due to RC-time constants and op-amp poles. This assumption leads to an efficient computer

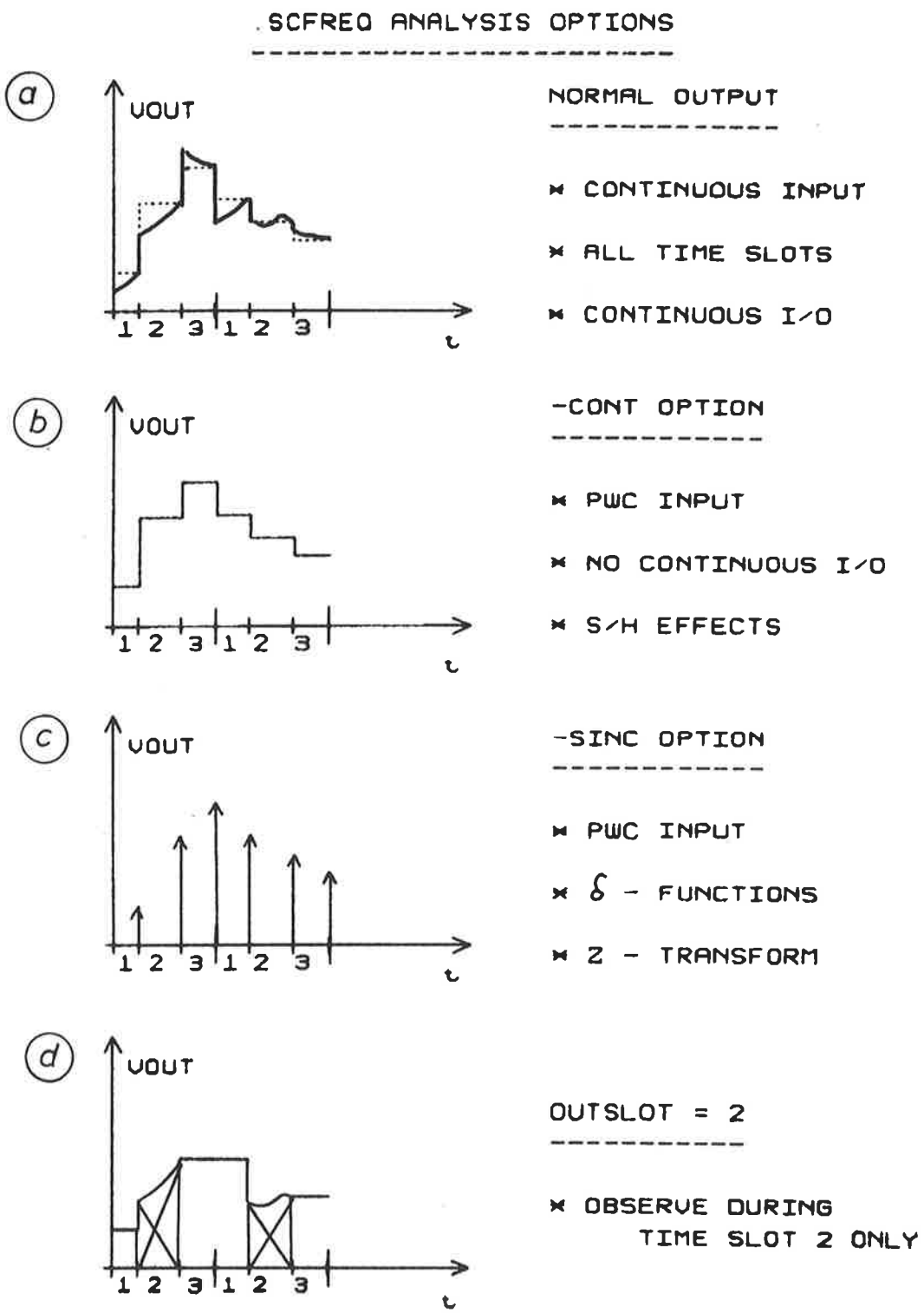
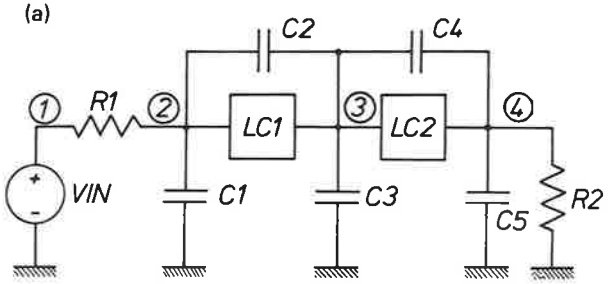


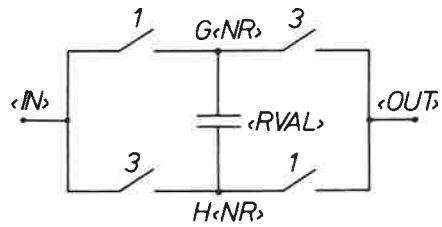
Fig. 2 Different analysis options in the frequency domain.

(a)

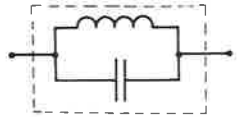


(b)

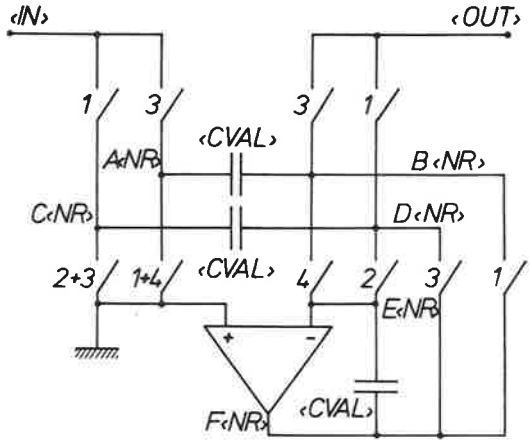
RESISTOR



(c)



LC - RESONATOR



(d)

```
;
; CIRCUIT DESCRIPTION
;
VIN 1 0 1
CALL RESISTOR(1,1,2,1.661P)
CALL RESISTOR(2,4,0,1.661P)
CALL RESONATOR(1,2,3,1P)
CALL RESONATOR(2,4,3,1.577P)
C1 2 0 9.382P
C2 2 3 1.763P
C3 3 0 14.382P
C4 3 4 6.929P
C5 4 0 6.162P
;
; CLOCKING
;
INPUT CL1 TIME=1 2 CYC=4
INPUT CL2 TIME=2 3 CYC=4
INPUT CL3 TIME=3 4 CYC
INPUT CL4 TIME=1 4 CYC IC=1
INPUT CL14 TIME=2 4 CYC=4 IC=1
INPUT CL23 TIME=2 4 CYC=4
;
; CONTROL CARDS
;
.SCFREQ NLIN=100 FSTART=0 &
FSTOP=32KHZ FSAMPLE=32KHZ AMPL
.SENS NODE=B1
PRINT 4
.END
```

(e)

```
$MACRO RESISTOR(‹NR›,‹IN›,‹OUT›,‹RVAL›)
;
;  RESISTOR ‹NR›
;
CE‹NR› G‹NR› H‹NR› ‹RVAL›
S2K‹NR› ‹IN› G‹NR› CL1 0
S2L‹NR› ‹IN› H‹NR› CL3 0
S2M‹NR› ‹OUT› G‹NR› CL3 0
S2N‹NR› ‹OUT› H‹NR› CL1 0
$END RESISTOR
```

(f)

```
$MACRO RESONATOR(‹NR›,‹IN›,‹OUT›,‹CVAL›)
;
;  LC-RESONATOR ‹NR›
;
XVA‹NR› F‹NR› 0 0 E‹NR› 1K
CB‹NR› A‹NR› B‹NR› ‹CVAL›
CC‹NR› C‹NR› D‹NR› ‹CVAL›
CD‹NR› E‹NR› F‹NR› ‹CVAL›
S2A‹NR› ‹IN› C‹NR› CL1 0
S2B‹NR› ‹IN› A‹NR› CL3 0
S2C‹NR› ‹OUT› B‹NR› CL3 0
S2D‹NR› ‹OUT› D‹NR› CL1 0
S2E‹NR› C‹NR› 0 CL23 0
S2F‹NR› A‹NR› 0 CL14 0
S2G‹NR› B‹NR› E‹NR› CL4 0
S2H‹NR› D‹NR› E‹NR› CL2 0
S2I‹NR› D‹NR› F‹NR› CL3 0
S2J‹NR› B‹NR› F‹NR› CL1 0
$END RESONATOR
```

Fig. 3 Fifth order elliptic lowpass filter according to ref. [13]. (a) analog reference filter; (b) SC equivalent resistor; (c) SC equivalent resonator; (d) MDL input description of the whole circuit; (e) macro description of the resistor block in (b); (f) macro description of the resonator block in (c).

calculation. However the assumption is not appropriate for noise transfer functions. The noise in all the higher bands is folded back into the base band. So the attentuation of the noise in higher frequency bands due to transient effects of resistance in switches and because of the finite bandwidth op-amps should be taken into account. A method which is compatible with the MNA method and which does not have these restrictions is presented in refs. [9] and [10]. An efficient computer algorithm is made if it is assumed that the equilibrium principle holds. This equilibrium principle requires that with zero input the circuit reaches equilibrium during each phase starting from arbitrary initial voltages on the capacitors at the beginning of the phase. In other words all time constants must be much smaller than the duration of the phase. At this moment work is being done at Leuven to get rid of this restriction.

3. The present DIANA.SC structure

In the preceding paragraphs a summary of the fundamentals of an efficient computer aided analysis technique for switched-capacitor circuits is given. By making use of all the above mentioned techniques, the DIANA-program has been developed to a complete top-down analysis system for switched capacitor circuits.

The DIANA package consists of three programs:

1. MDL (macro description language). By making use of the MDL language a hierarchical description can be made by using macros. The MDL input description is expanded into the DIANA input language. Hereafter an analysis can be done in the DIANA program.

2. DIANA is the simulation program itself.

3. PPR (post processor). The simulation results of DIANA can be stored for later processing by the PPR program. This program allows one to make line printer plots, printouts and drawings.

The DIANA program itself consists of two parts. The first part is the mixed-mode part, DIANA.MM, which allows for a mixed mode circuit-, timing- and logical analysis[11,12] of MOSLSI circuits. The second part, DIANA.SC, is the SC-analysis part.

In the DIANA.SC program there are three analysis levels which are shown in Fig. 1: a top-, intermediate- and bottom level.

1. **TOP level.** The highest level of abstraction (and calculation efficiency) is the top level. In this analysis mode it is assumed that there are no time constants due to resistors and op-amp poles.

2. **INTERMEDIATE level.** Resistors and op-amp poles can be included at the intermediate level if the equilibrium principle (Sec.5) is valid

3. **DOWN level.** At the down level MOS transistors and non-linear junction capacitors can be used and this only in the time domain analysis.

At all levels, ideal switches, capacitors, independent voltage- and charge sources and dependent sources VCVS, QCVS, QCQS and VCQS can be used. All four dependent sources have a finite gain. All switches are controlled by external Boolean clock variables $\varnothing_i$. All clock signals must be T-periodic, with N time slots (phases) in one period of duration T. In DIANA there is no restriction on the number of time slots N. There is no restriction on the circuit topology, except for trivial cases such as loops of voltage sources and closed switches and cut sets of charge sources and open switches.

The calculations are performed directly in the frequency domain. This is more efficient than the early method[3] with the FPR program which used FFTs of impulse responses. Therefore the FPR program is not used any more at this moment.

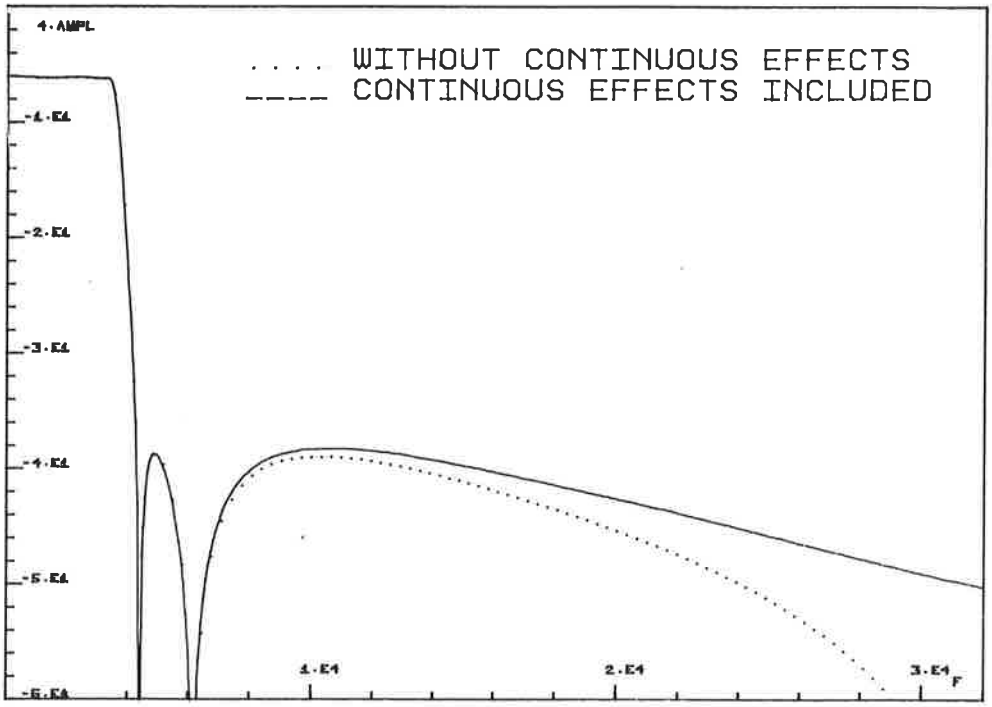


Fig. 4 Amplitude response of the fifth order filter in Fig. 3.

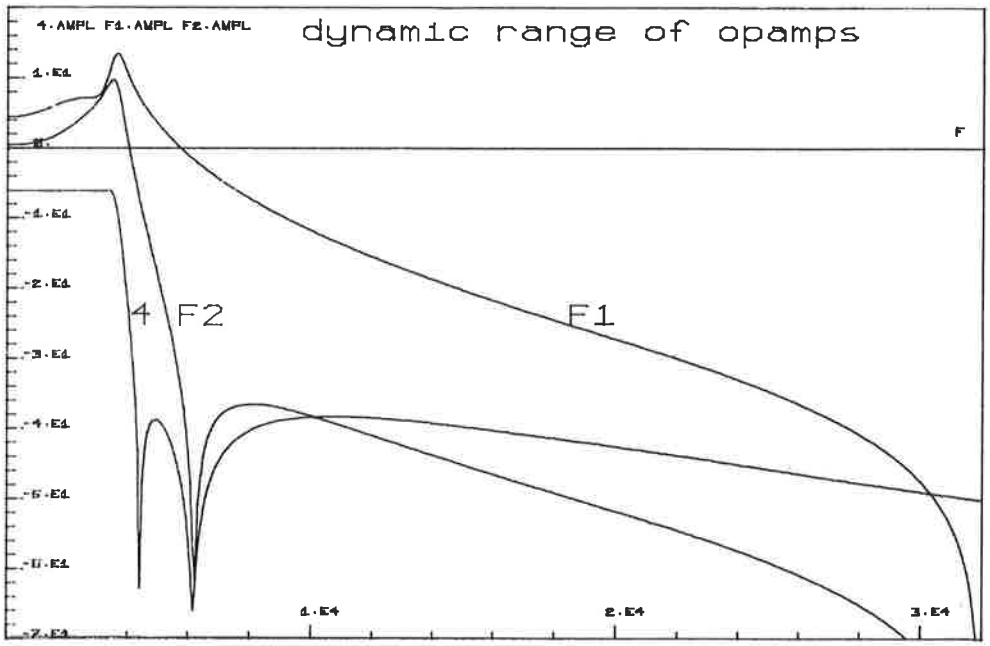


Fig. 5 Study of the dynamic range of the filter in Fig. 3.

4. Top level analysis

The top level analysis of a SC-filter is usually applied as the first analysis of the filter concept, to see if the requirements in the time- and frequency domain can be met.

The time domain analysis mode can be done in an efficient way using one calculation per timeslot[3] (".SCTIME"-card). So the analysis can be done from one equilibrium state to the next one. Examples of this mode can be found in ref. [3].

In contrast with classical filters, SC-circuits can be excited and observed in different ways. In contrast with most other SC-analysis programs, different observation modes are possible in DIANA. At the top level frequency domain (".SCFREQ") these observations modes are specified with options in the .SCFREQ card as summarised in Fig. 2.

1. **CONT, SINC options.** The default output of DIANA includes continuous input-output couplings and this over all the timeslots (Fig. 2(a)). The transfer function is analysed with the full eqn. (2).
2. **-CONT, SINC options.** By using the "-CONT" option the input is assumed to be piecewise constant (Fig. 2(b)). With this assumption continuous input-output couplings have no effect. Only the sample and hold effects are taken into account. This calculation is done with eqn. (2) where the second term at the right-hand side is omitted.

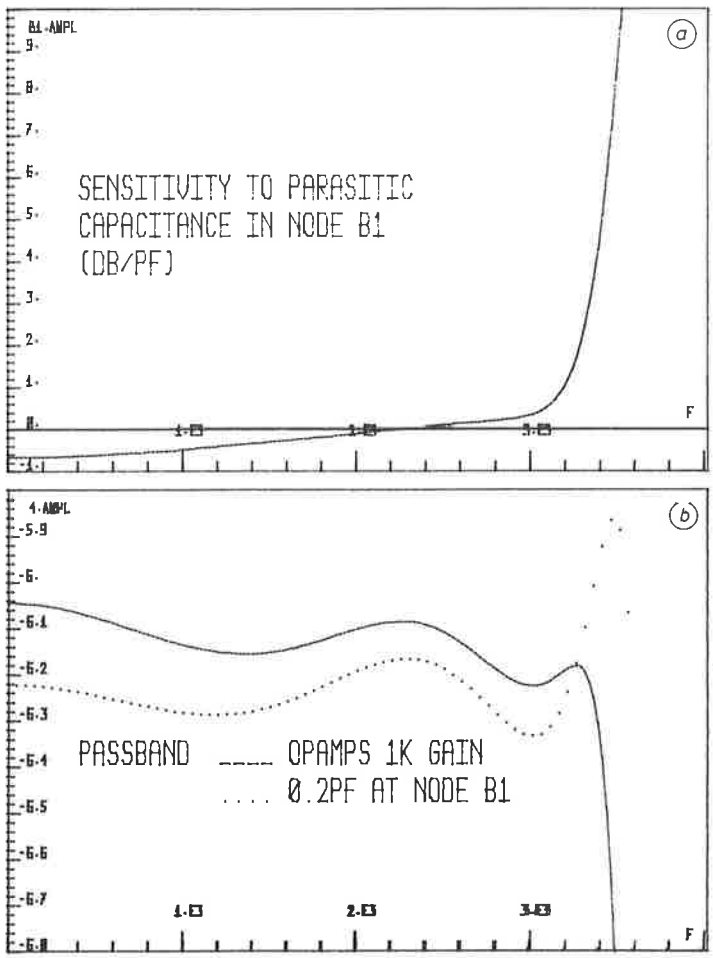


Fig. 6 (a) Amplitude sensitivity to parasitic node capacitance. (b) Disturbance of the passband amplitude by a parasitic capacitance.

3. **-CONT, -SINC options.** By using the "-SINC" option even the sample and hold effects can be suppressed so that a series of delta impulses is obtained which can be analysed by the z-domain analysis (Fig. 2(c)). This can be used to verify if the filter function corresponds to what was produced by the z-domain synthesis methods. This transfer function is analysed without the second term at the right-hand side of eqn. (2) and with

$$\nu_k(\rho) = (t_{k+1} - t_k) / T \qquad \text{(4)}$$

4. **OUTSLOT option.** With the "OUTSLOT" option (Fig. 2(d)) the output can be sampled during selected time slots and held during the other timeslots. The "OUTSLOT" option together, perhaps, with the "-CONT" and "-SINC" options can be used to study the transfer functions to the output filters in certain time slots. This can be of interest if the filter is followed by another SC-filter which samples the output of the previous filter only during parts of the time slots.

5. **BAND option.** When applying a sinusoidal input signal to a SC-circuit, a multitude of output sinusoidal components in different frequency bands will occur due to the sampling process. These effects can be studied in the aliasing analysis. In DIANA the frequency spectrum is divided into bands which have a width of half the sample frequency. When analysing the transfer function from a signal at one frequency, Ω, to another frequency, ω, as indicated in eqn. (2), the results correspond to measurements with a frequency selective voltmeter which measures the output signal only at the frequency ω. In the transfer function analysis the input signal frequency and the observed output frequency are the same.

In order to obtain information about the accuracy by which element values must be realised or for optimisation purposes, a sensitivity analysis of the transfer function to capacitor values and op-amp gains is necessary. This has been efficiently built into the DIANA program by making use of the adjoint network concept[5] which uses the transpose of the reduced z-domain MNA matrix.[7,8]

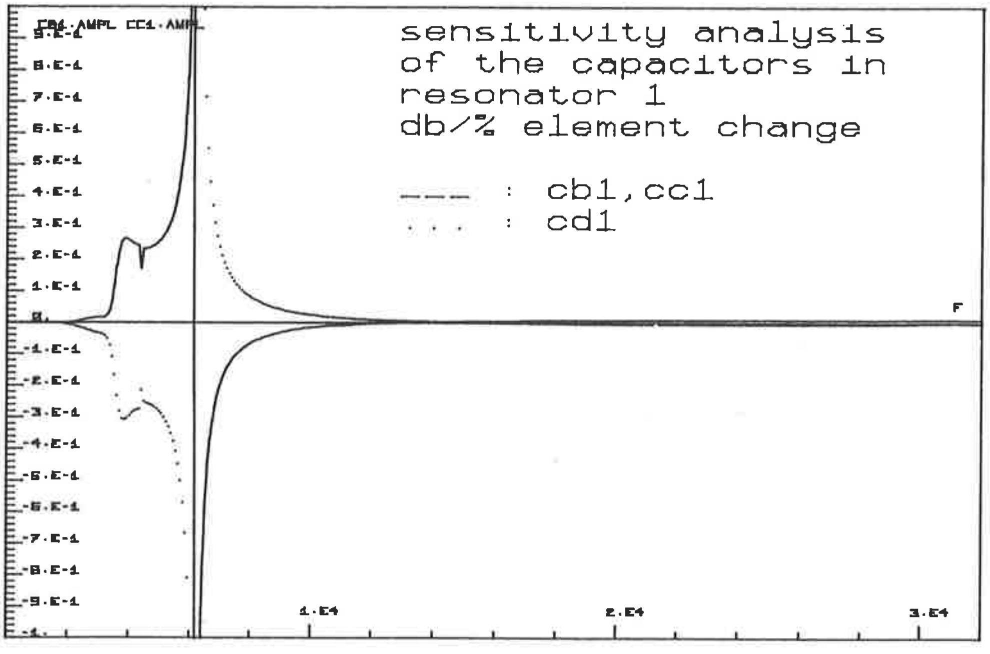


Fig. 7 Amplitude sensitivity to capacitors.

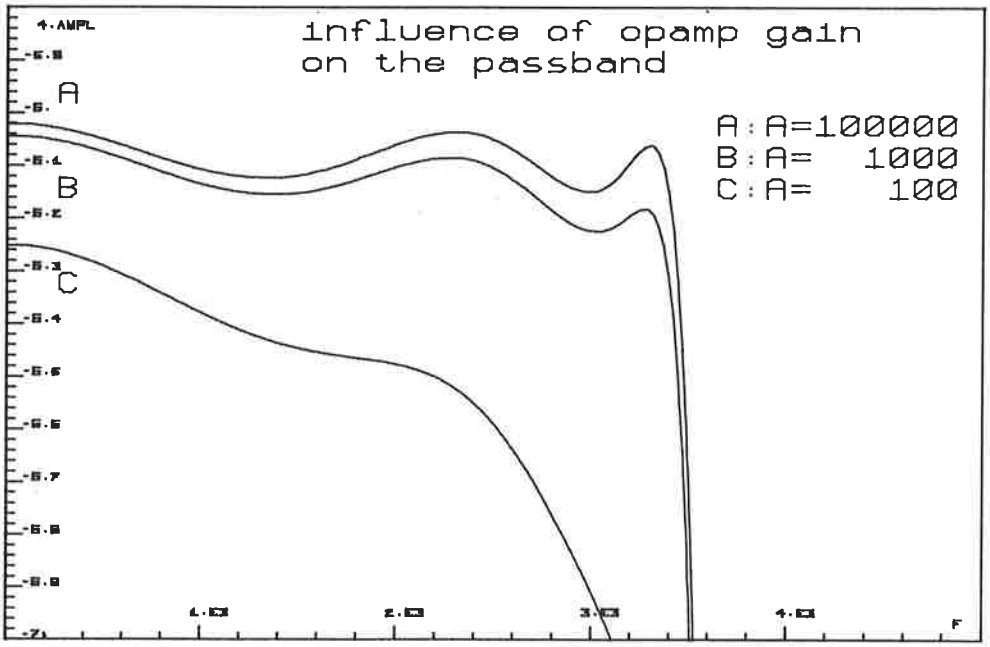


Fig. 8 Influence of the op-amp gain in the passband.

Because switched capacitor circuits are usually implemented on-chip, there is nearly always a certain parasitic capacitance at each node. It is therefore important for the filter designer to study how the filter response is degraded by these parasitic capacitances. With the sensitivity analysis to parasitic node capacitances in DIANA the designer receives information on how sensitive his filter implementation is.

In the next sections some case studies will illustrate the input-output features and the options explained above.

4.1 Top level analysis of a fifth order filter

In this case study a top level DIANA analysis of a modular fifth order elliptic low pass filter according to the theory of Nossek and Temes[13] for the SC-filter synthesis is shown. The design procedure starts from an analog reference filter as shown in Fig. 3(a). By making use of the bilinear s-to-z transformation resistors are transformed into the circuit of Fig. 3(b), while LC resonators are transformed into the circuits of Fig. 3(c). Capacitors remain capacitors. The topology of the SC-filter is the same as the reference filter. The SC-filter is controlled by four-phase clocks.[13]

First the input features are demonstrated. This circuit contains some repetition and therefore it can be described hierarchically with the MDL language. In Fig. 3(e) the "SC-resistor" is written as a $MACRO in the MDL language. <NR> is the number of the resistor. <IN> and <OUT> are the terminals of the resistor. <RVAL> is the value. Notice the description of the capacitors CE<NR> and the four two-node switches: S2K<NR> . . . S2N<NR>. The description of the LC resonator is given in Fig. 3(f). The switches are clocked by clocks CL1 to CL4 and combined clocks such as CL14 and CL23. Now the whole circuit description reduces to the calls of the several macros corresponding to the circuit topology as shown in Fig. 3(d). The description of the clock signals is given with the "INPUT" statements.

In the ".SCFREQ" card an analysis over 400 frequency points from DC up to 32 kHz is specified. Figure 4 shows the transfer function including continuous input-output effects (default). If the input is assumed to be piecewise constant the continuous input-output coupling is not taken into account ("-CONT" option) and the dotted curve is obtained. This difference corresponds to the difference that was obtained with a similar third order filter in ref. [14]. The measured results of ref. [14] deviate from the theoretical results because of the continuous input-output coupling effects that are not taken into account in the theoretical results of ref. [14]. Figure 5 shows a study of the dynamic range of the two op-amps.

With the ".SENS" card a sensitivity analysis of the transfer function to the parasitic capacitance in node B1 is requested. In Fig. 6 a study of the transfer function sensitivity to parasitic capacitors in node B1 is shown. There is a sensitivity of ~0.7dB/pF in the passband. This deviation can also be seen when a capacitor of 0.2pF (20% of the smallest capacitor) is

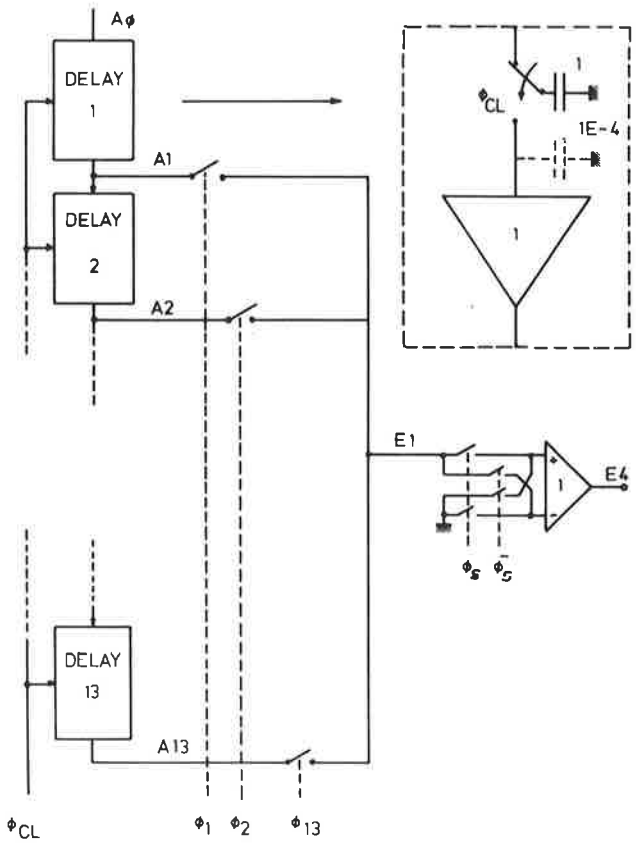


Fig. 9 Lowpass filter with transfer function depending only on timing ref. [16].

added in node B1. Now a passband droop is seen to degrade the passband ripple. An analogous effect is mentioned in ref. [13] in the measurements of a prototype of this filter. Perhaps this is due to the parasitic capacitances in the nodes.

Figure 7 shows the transfer function sensitivity characteristics to capacitors in the first resonator. In Fig. 8 a study of the passband for different op-amp gains is shown.

The original z-domain MNA matrix had a dimension of 204. By the matrix compaction algorithm of DIANA this big matrix could be reduced to a dimension of 16. The matrix

set-up, re-ordering and compaction of the filter as described in Fig. 3(d) took 14.2 sec. on a VAX 11/780. The CPU-time for the frequency analysis (after compaction) over 400 frequency points took 20.9 sec. If the compaction process is left out, the matrix set-up and re-ordering takes 22.3 sec. and the frequency analysis takes 142.5 sec. Notice that a gain of 6.8× is achieved in the frequency analysis time at no expense to compaction (and re-order) time! The difference in compaction-, matrix set-up- and re-ordering time is due to the re-ordering of smaller submatrices in the case of compaction.

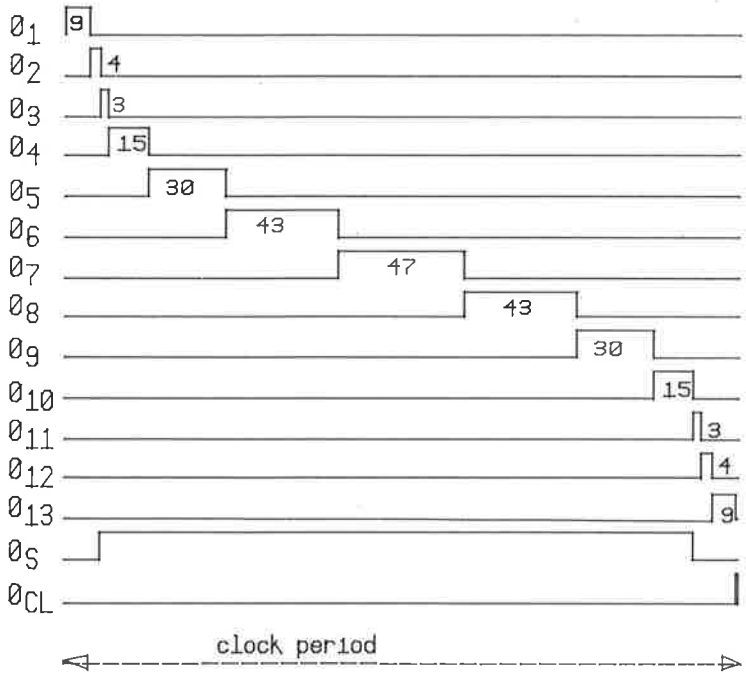


Fig. 10 Timing diagram of the filter in Fig. 9.

4.2 Top level analysis of a transversal filter whose coefficients depend only on timing.

The DIANA.SC program allows for the analysis of circuits with multiple clock phases and arbitrary duty cycles. Therefore it is possible also to analyse unconventional filters. The following example was used to illustrate the multi-time slot and arbitrary duty cycle operation of DIANA.SC to illustrate how compaction results in an efficient calculation.

In ref. [16] Tsividis proposed a new filter implementation where the transfer function coefficients are determined only by the timing. Figure 9 shows a schematic diagram of an FIR filter according to the principles in ref. [16]. The filter consists of a delay clocked by $\varnothing_{CL}$. An element of the delay line is realised as an SC-circuit as shown in Fig. 9. The coefficients at each tap of the delay line are realised by closing a switch from A_i to E_i during a certain time interval under control of a clock $\varnothing_i$. The duty cycle of the clock $\varnothing_i$ determines the coefficient value for that tap. The sign of the coefficient is determined by the clock $\varnothing_s$.

The following 13-tap lowpass filter has been designed with the program in ref. [17] for equi-ripple in the passband from 0 to $0.08F_s$ and in the stopband from $0.16F_s$ to $0.5F_s$. The weights in the stopband and the passband were both taken to be equal to 1. This results in 0.5606 dB passband ripple and a −23.52 dB rejection in the stopband. If there is a resolution of 1/256 of the basic clock frequency F_s, the coefficients must be rounded to fit in the clocking scheme. In Fig. 11 the dotted curve gives the response of the 'classical' FIR filter implementation with rounded coefficients. These coefficients are realised in the filter of Fig. 9

if the clocking sequence of Fig. 10 is applied. The full line in Fig. 11 gives the response of this filter (Fig. 9) as simulated with DIANA. MDL was used for the modular input description. This circuit contains 14 time slots and resulted in a z-domain MNA matrix of dimension 896. Due to the matrix compaction algorithm it could be reduced to a dimension of 41. The VAX CPU time over 500 frequency points was 247.6 sec.

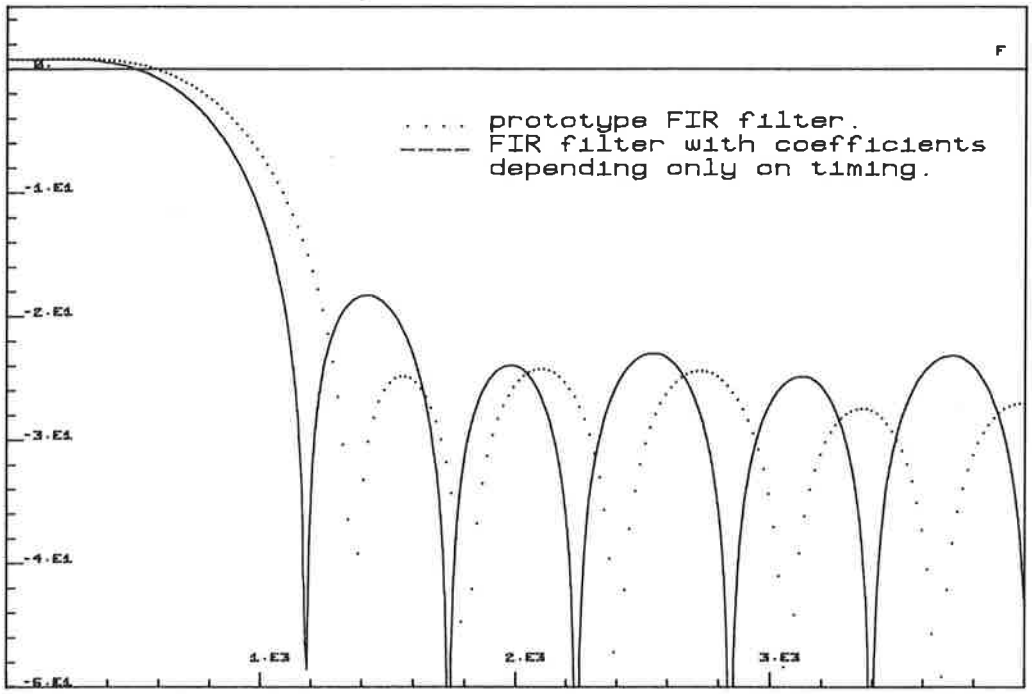


Fig. 11 Frequency response of the reference FIR filter and the FIR filter according to Fig. 9.

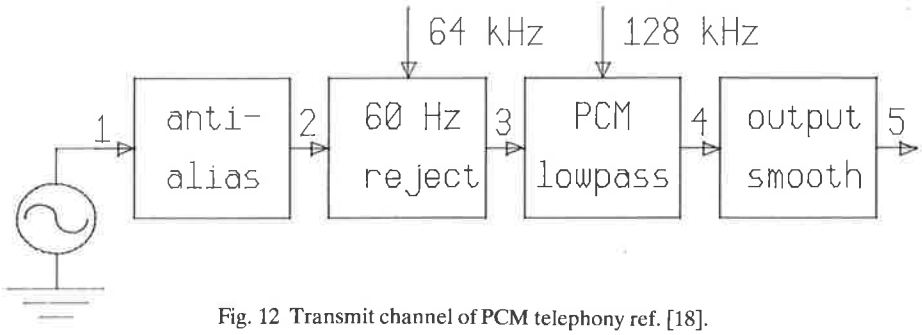


Fig. 12 Transmit channel of PCM telephony ref. [18].

5. Intermediate level analysis

In a further stage the designer wants to investigate the influence of finite op-amp bandwidth and switch resistances on the frequency response. This is important also for noise calculations. Under the assumption of the equilibrium principle[9] this analysis can be done at the intermediate level of DIANA.

The additional elements allowed at this level are resistors and macro models for non-ideal

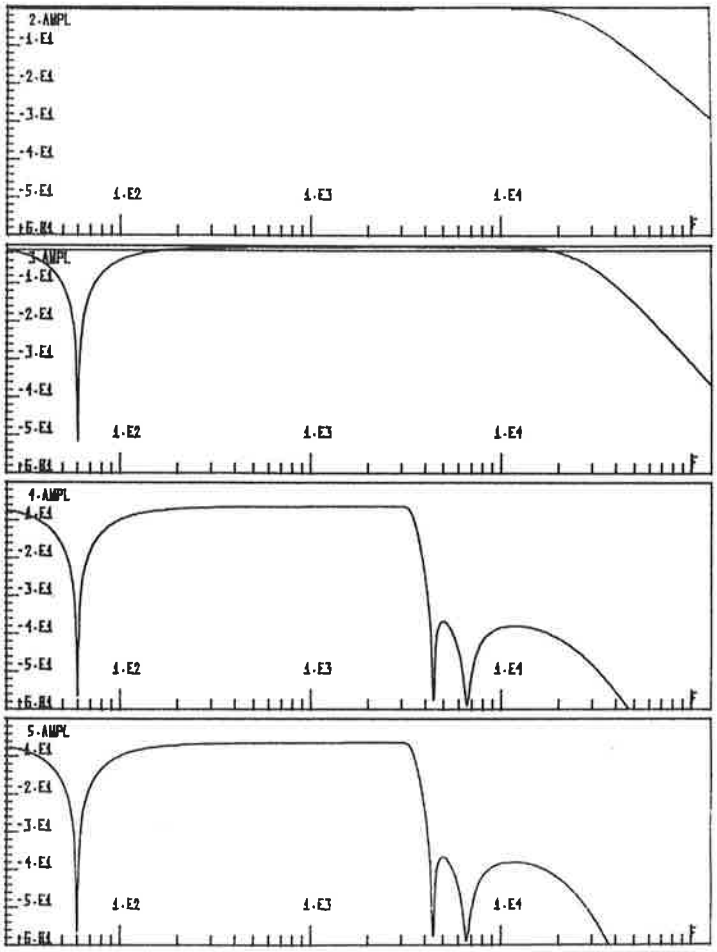


Fig. 13 Amplitude response at the different points in the channel of Fig. 12.

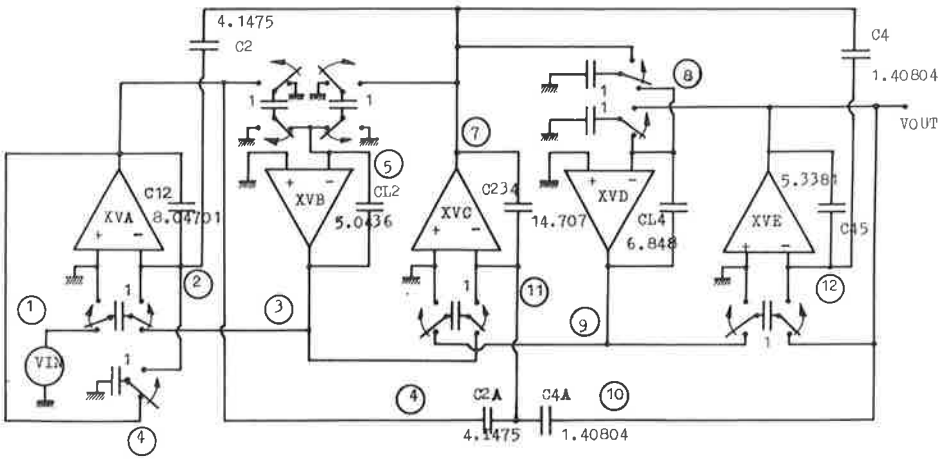


Fig. 14 Fifth order elliptic lowpass filter.

op-amps. As shown in Fig. 1, this macro model can include output conductance, a unity gain frequency and a complex pole pair, finite gain, input parasitic capacitances and a noise source.

When specifying one or more resistors and/or built-in macro models for op-amps, the DIANA.SC program in the frequency domain (".SCFREQ" card) is automatically directed into the intermediate level.

For the noise calculations a similar aliasing analysis can be done as on the top level analysis but now with the inclusion of resistors and non-ideal op-amps. Such noise transfer functions must be calculated from the noise sources to the output.

The time domain analysis at the intermediate level is done (".TRAN" card) by the usual circuit analysis mode of DIANA.

5.1 Intermediate analysis of a channel filter for PCM telephony applications

Figure 12 shows the transmit channel of a PCM filter. It consists of the cascade of a second order analog Sallen and Key anti-aliasing filter,[18] a 60Hz rejection SC-filter,[18] a fifth order PCM low pass SC-filter[19] (Fig. 14), and a second order analog Sallen and Key filter for smoothing. This channel consists of a mixture of analog filters and SC-filters. The SC-filters are analysed including switch resistances of 10 kΩ and op-amps with a DC gain of 1000 and a pole at 500 kHz. Because of the resistors in the two Sallen and Key filters and the resistors

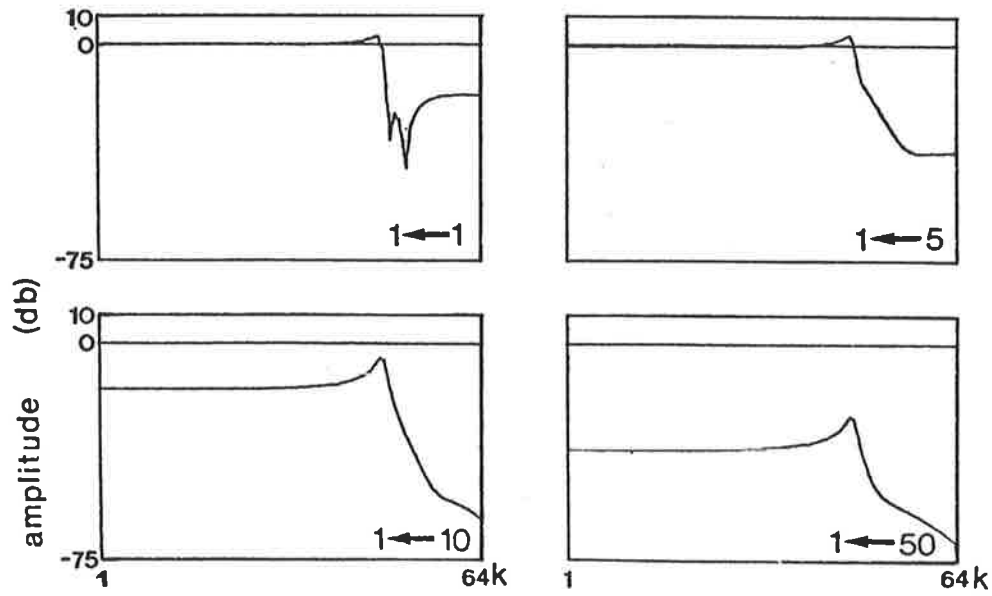


Fig. 15 Noise transfer functions from op-amp XVA to the output of the filter in Fig. 14.

included in switches and op-amp poles there will be transient effects and therefore this filter cannot be analysed at the top level. The analysis of this filter at the intermediate level with the responses in the different parts of the channel are shown in Fig. 13 in full lines. The total VAX CPU time of an analysis over 400 frequency points was 16 min. 36.8 sec.

5.2 Analysis of noise transfer functions of a PCM lowpass filter

As stated in ref. [5], the noise of SC-circuits is the result of an infinite sum of noise values, due to the folding of noise from the higher frequency bands in to the base-band. This summation is truncated by bandwidth limitations imposed by the op-amps and the RC time constants. The mechanism of noise transfer is demonstrated in Fig. 15 for the PCM lowpass of the previous

case study, where the noise transfer from one operational amplifier noise source to the output node is calculated (assuming only white noise for simplicity). The values of the noise transferred from several frequency bands to the base band is shown. The effect of bandwidth limitation is clearly demonstrated. The total noise value can then be calculated, taking the squared sum of all these noise contributions. Improved automatic computation of this sum and of all other noise effects such as 1/f noise are in progress.

6. Bottom level analysis

At the bottom level analysis nonlinear capacitors and MOS transistors can be included. Here only time domain transient analysis (".TRAN" card) is possible. At this level a mixed mode analysis of logic-, or timing gates and a SC-circuit is also possible. Various examples of this operation mode were demonstrated in ref. [3].

7. Current developments in the DIANA-program

At the moment an algebraic analysis is completed by the authors to remove the stringent requirement of the equilibrium principle at the intermediate level. In the near future this new intermediate level analysis will be implemented in DIANA. The noise analysis will then be automated.

For the analysis of nonlinear effects in the frequency domain a distortion analysis using Volterra series for SC-circuits[15] is being built into the DIANA.SC program.

The top level time domain analysis is being optimised by making use of the compacted z-domain MNA matrix. So a CPU time saving is achieved compared with the present implementation in DIANA.

A full top-down analysis of digital filters for MOSLSI implemetations is currently under development by the authors. A top level analysis comparable to the top level analysis in DIANA.SC has already been completed.

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