COMPUTER AIDED DESIGN OF SWITCHED CAPACITOR CIRCUITS USING THE DIANA PROGRAM

H. De Man
L. Claesen
J. Rabaey
J. Vandewalle
Katholieke Universiteit Leuven
Laboratorium ESAT
Kardinaal Mercierlaan 94
3030 Heverlee, Belgium

1) The DIANA program : a general overview.

The DIANA program is basically a mixed-mode simulation program for MOSLSI circuits.
Mixed-mode refers to the fact that circuits can be analyzed at different levels of abstraction without having to change program or description language.
Basically the program is oriented towards DIgital as well as ANAlog MOS circuits.

The ANAlog part is specifically oriented towards switched capacitor (SC) circuits whereby time, frequency sensitivity and noise operation is possible, ranging from idealized networks (top-design) all the way down to detailed MOS transistor networks (down-design) such as full n-MOS and CMOS opamps (the latter only in the time domain).

The DIgital part allows for simultaneous simulation in the time domain of MOS circuits described at the circuit, timing and logic level.

The description language of DIANA is SPICE like and can be generated from a Macro Description Language which allows for a compact nested hierarchical description for circuits which consist of an interconnection of a large number of identical (parametrizable) blocks as is often the case for LSI and VLSI networks.

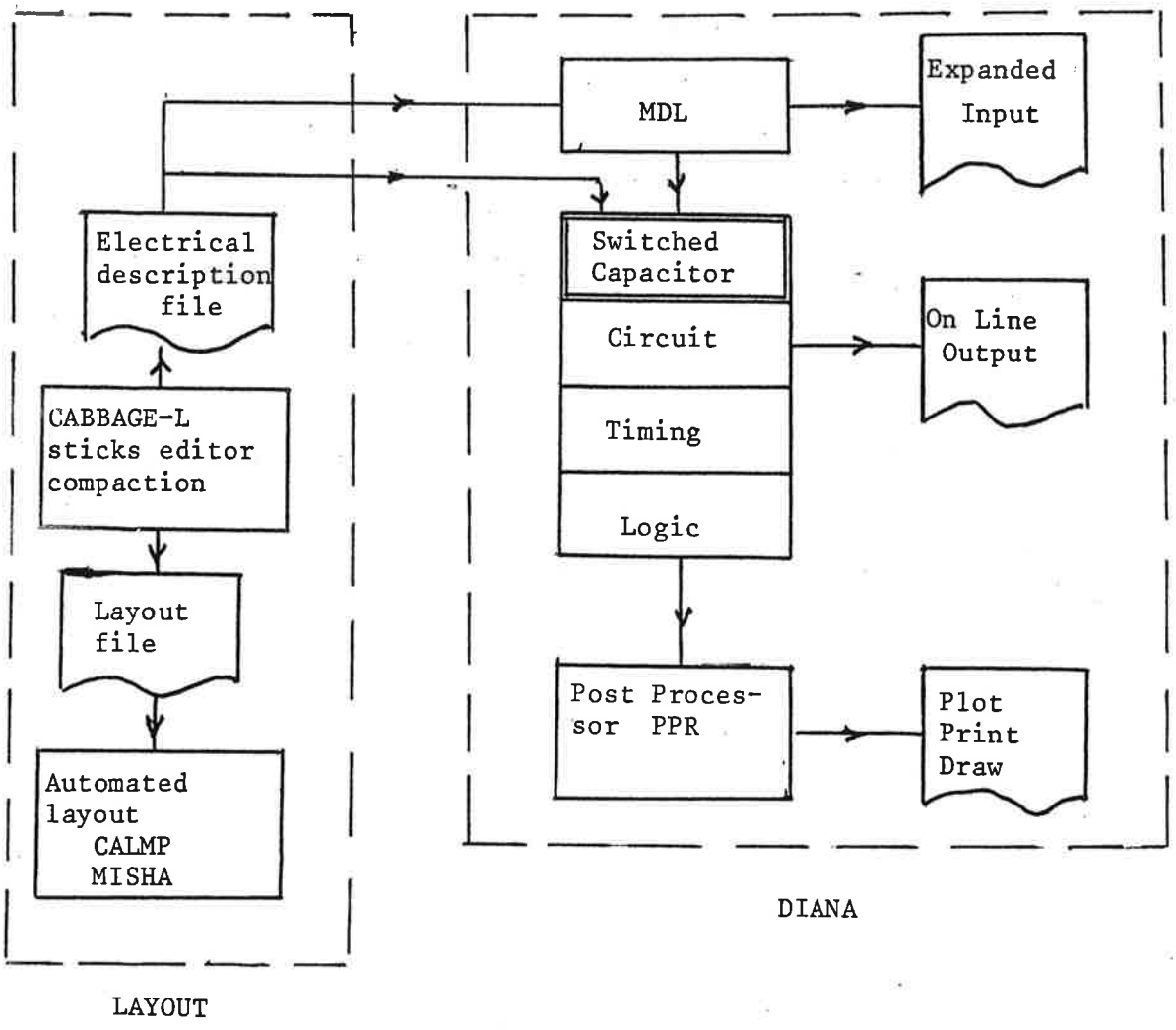


Fig. 1

Fig. 1. gives a general top-view of the DIANA program at the time of this writing.
Notice that, for n-MOS, circuit files can be immediately extracted from layout. The program has a limited on-line output facility (terminal) and an extensive output facility for printing, plotting and drawing by a Post Processing module PPR.

In this section we will mainly concentrate on the Switched Capacitor analysis feature of the program.
For a detailed description of the complete program the reader is referred to [1] [2] [3] [4] which are included in the notes. It is to be noted that, since the time [4] has been published, many improvements and extensions have been made to the sc-mode of the program as already discussed in the previous lectures.

2. The DIANA program for s.c. applications.

2.1. Once over lightly.

Based on the work presented in [4] [5] [6] [7], DIANA allows for the analysis of arbitrary switched capacitor networks at three different levels of abstraction : top, intermediate and down. Hereby time, frequency, sensitivity and noise calculations are possible.
Table 1 below summarizes the different possibilities. The .XXXX..... statements correspond to CONTROLCARDS (See manual, § 3) controlling the analysis mode described. Notice that the three abstraction levels correspond to a "top-down design methodology" which is normally used to design complex systems.

S.c. design usually starts by deriving a network consisting of ideal (time constant free) switches-capacitors-op-amps to satisfy a given frequency-phase or time domain response.
Table 1 illustrates clearly how in this TOP mode behavior in time (.SCTIME), frequency (.SCFREQ) and tolerance (.SENS) space can be done.

Once a satisfactory "ideal sc network" has been defined, it is possible, at the INTERMEDIATE level, to add "time-constant" effects to the network (real switches, real-opamps with finite poles, zero's, output impedance etc...) and to reverify frequency (.SCFREQ) behavior. It is then also possible to compute (using the adjoint network concept [7] , all noise transfer functions (including aliasing effects), to verify the noise behavior of the network (.NOISE). It is also possible using the .TRAN option to integrate the network in the time domain to check, for example, high frequency effects (incomplete charging) and / or clockfeedthrough effects which are often very difficult to evaluate otherwise.

TABLE 1 : DIANA FOR SWITCHED CAPACITOR NETWORKS

ABSTRACTION LEVEL	ANALYSIS MODE	DESCRIPTION	APPLICATIONS
TOP	RESISTORFREE T-PERIODIC SC NETWORK (NO RC TIME CONSTANTS, FINITE GAIN IDEAL AMPLIFIERS)		
	.SC TIME	time domain : 1 analysis per clock phase (time slot)	impulse response, nonlinearities, offset, leakage currents
	.SCFREQ	amplitude&phase vs. frequency including band to band response	stray parasitics, aliasing, S/H effects, clock-duty cycle, continuous coupling ...
	.SENS	amplitude & phase sensitivity to capacitor, opamp gain and stray capacitance to ground	design optimization, stray effects, tolerance assignment ...
INTERMEDIATE	SC NETWORKS INCLUDING RESISTORS, OPAMP-POLES, OUTPUT IMPEDANCE, WHITE AND 1/f NOISE SOURCES		
	.SCFREQ	idem as top but including time constants and op-amp poles	Q degradation, peaking and drooping effects, high frequency behavior
	.NDISE	computation and summation* of noise transfer functions of small noise sources (R's and op-amps)	noise prediction and optimization
	.TRAN	time domain transient analysis including RC and first order MOS model	high frequency limitation, clock - feedthrough
DOWN	.TRAN	FULL CIRCUIT ANALYSIS INCLUDING n AND p-MOS TRANSISTORS	op-amp design, stability op-amps modeling, logic design ...

*in preparation at the time of writing.

Using the circuit mode of DIANA it is also possible to simulate the filter in the time domain (.TRAN) at the MOS transistor level and even down to the driving logic if it is an adaptive filter. This option is very useful also, for example, to derive, from a detailed circuit analysis, op-amp models to be used in the INTERMEDIATE mode.

In contrast to other existing simulators DIANA is believed to be the only one offering this full top-down aid in one package.
In what follows the different modes will be commented and illustrated by several examples.

2.2. TOP-level analysis of s.c. networks.

Essential to TOP-level design is that no resistors nor amplifier bandwidth limitations are allowed in the input description. It is therefore implicitly assumed that the network reaches a new equilibrium state immediately after a clock transition such that, instead of currents $i_j(t)$, charges $q_{j,k}(t) = \int_{t_k}^{t \in \Delta_k} i_j(t)\,dt$ are used in Kirchoff's "current" law. Therefore all "current" sources are to be considered as charge sources (see also [4], [8]).
In what follows we indicate what kind of network elements are allowed and how they are to be used in the different modes of simulation.
For syntax details the reader is referred to the DIANA manual [3].

2.2.1. .SC TIME mode.

Control statement : .SCTIME NCYC= (FSAMPLE=))

Allowed network elements :

- ideal switches driven by T-periodical (CYClic) clocks (INPUT)*
- capacitors (linear or nonlinear MOS junction capacitances)
- voltage and charge sources
- four dependent linear sources (VCVS, QCVS, VCQS, QCQS)

Type of analysis : The T-periodical clocks (INPUT) driving the switches divide the period T into N time slots $\Delta_k = t_{k+1} - t_k$ with duty cycle $d_k = \Delta_k / T$
The network is analyzed once per time slot at each t_k over NCYC periods. Sources are sampled at each t_k. The charge source value at t_k is the integral of the current over the previous time slot Δ_{k-1} (e.g. to study the influence of leaking charge).

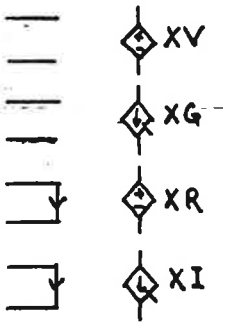
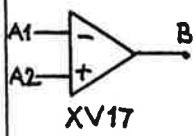
---

* Underlined words in capital characters correspond to DIANA syntax.

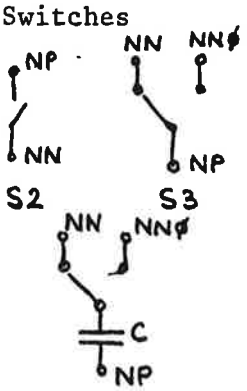
Basis : The sc network MNA equations are set-up and solved from one time slot to the next using charge conservation. See [5], equations (1) through (5), and Fig. 1, [5].

Allowed network elements : details.

Given below are the network elements which are allowed for .SC TIME analysis. We only indicate some essential points with respect to .SC TIME analysis. For more details about the network elements we refer to the DIANA manual [3], § 4.

Element	Remark
Capacitor 	C ..... NP(=) NN(=) VAL(=) Nonlinear MOS junction capacitances are also allowed. (See manual).
Voltage source 	DC source : V.....(NP(=) NN(=) VAL(=) time dependent : V..... NP(=) NN(=) INPUT=name In DIANA time dependent sources are defined by an INPUT statement [3], § 4II which allows it to be described as a piecewise linear function of time, a block wave or a superposition of sine-waves. See also below for switches.
Charge sources 	DC source : I..... NP(=) NN(=) VAL(=) time dependent : I..... NP(=) NN(=) INPUT=name Notice that in .SC TIME the "current" sources become charge sources as discussed before.
Amplifiers or dependent sources 	Four types given in 3 §4 I B are allowed but notice that all "currents" have to be interpreted as charges e.g. XV..... : VDVS XG..... : VDQS XR..... : QDVS XI..... : QDQS Example : op-amp, gain 1000  XV17 B 0 A2 A1 1000

Switches



S3 ... C(=)

No S4 available. S3 is either in NN or in NNØ (no intermediate open position)

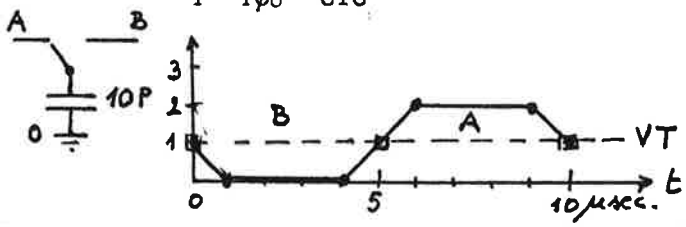
Several switches can be defined. They must be resistorfree (ideal) and controlled by T periodical clocks using the INPUT CYC definition for clocks.

DIANA has only voltage dependent clocks. Switching occurs when the controlling voltage between nodes NCP(=) and NCN(=) crosses the threshold voltage VT(=).

Thus a switching instant is defined when the controlling voltage defined by the INPUT statement equals the VT of the switch.

Example :

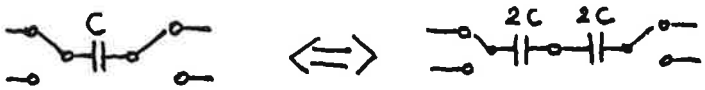
```
S3A  Ø  A  B  CL1  Ø  C = 1ØP  VT = 1
INPUT  CL1  1  Ø  Ø  1U  Ø  4U  2  6U  2  9U &
       1  1ØU  CYC
```



The following switch would have opposite phase :

```
S3B  Ø  A  B  Ø  CL1  C=1ØP  VT=-1
```

Further : 1) if non-overlapping clocks are to be used one must use S2 switches. Also notice that often a "double S3-C" branch occurs which can be modelled as shown below :



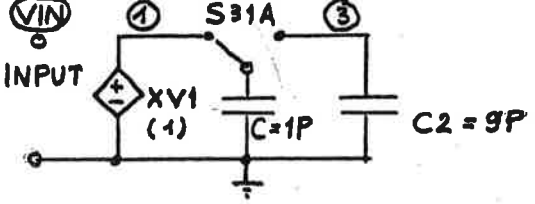
The use of S3-C switches is recommended (wherever possible) because it speeds up the execution time.

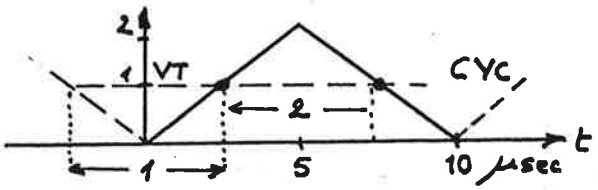
In .SCFREQ a "double S3-C" branch is called an S4 branch and can be used as an allowed networkelement

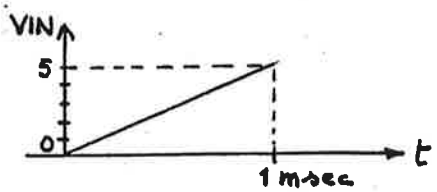
2) the optional statement (FSAMPLE=) in the .SC TIME statement overwrites the clockperiod for the switches and makes the period equal to $FSAMPLE^{-1}$.

Example : The following is a simple example of a switched capacitor "RC" equivalent driven by a ramp input. It clearly illustrates the input language and operation of the program.

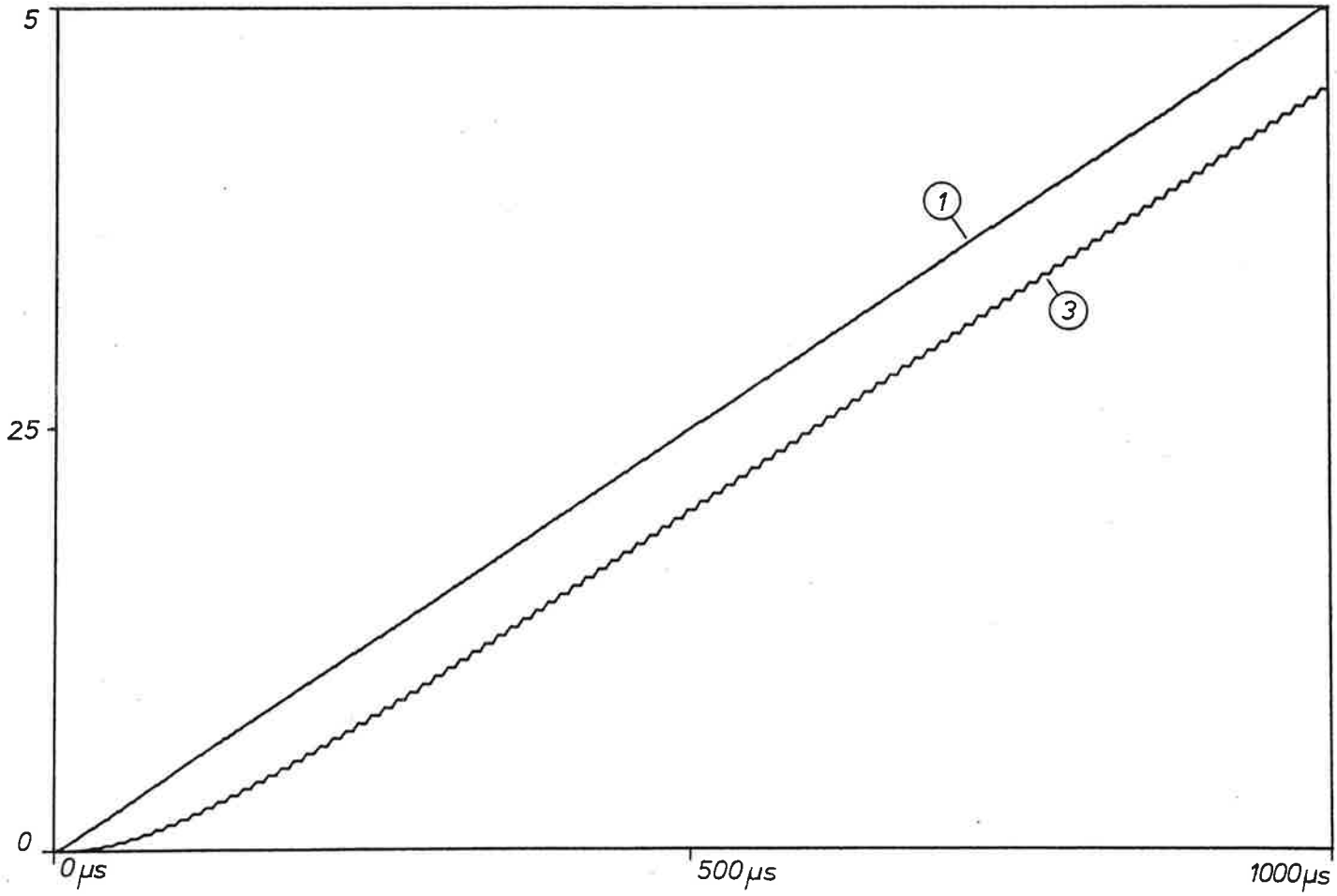
```
*************************************

  ESAT RC-LOW

*************************************

  .SCTIME NCYC=100 FSAMPLE=100KHZ
  INPUT VIN V-T=0 0 5 1M
  XV1 1 0 VIN 0 1
  C2 3 0 9P
  S31A 0 1 3 CL 0 VT=1 C=1P
  INPUT CL V-T=0 0 2 5U 0 10U CYC
  PRINT 3 1
  .OPTIONS STORE
  .END
```








```
  SWITCHED CAPACITOR DATA


            TIME DOMAIN ANALYSIS

            TIME SLOT
             ALL

            NUMBER OF CLOCK CYCLES NCYC=      100


  SWITCHED CAPACITOR SIMULATOR : TIME SLOT INFORMATION

            CLOCK PERIOD =  1.000E-05

            NR OF TIME SLOTS =  2
            OUTPUT OBSERVED IN TIME SLOT : ALL

            TIME SLOT SPECIFICATION
             SLOT  1      FROM -2.500E-06  TO  2.500E-06      DUTY =  5.000E-01
             SLOT  2      FROM  2.500E-06  TO  7.500E-06      DUTY =  5.000E-01
```



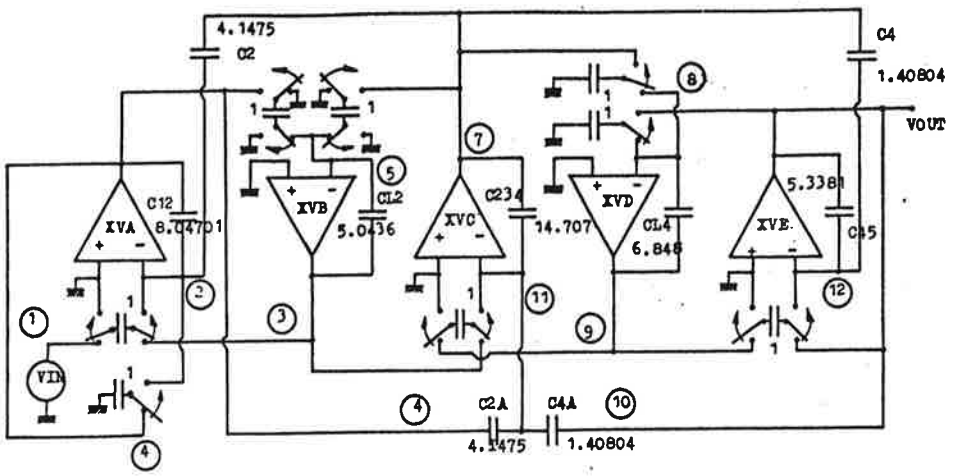
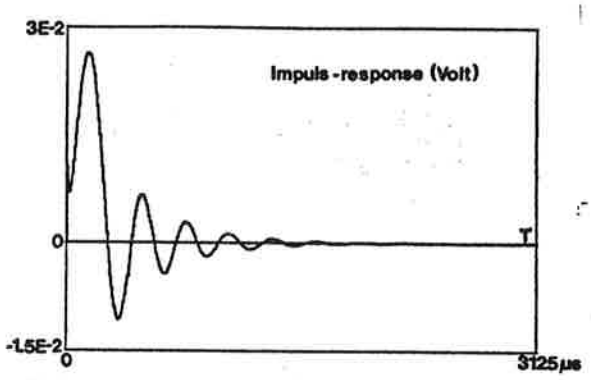


Fig. 2



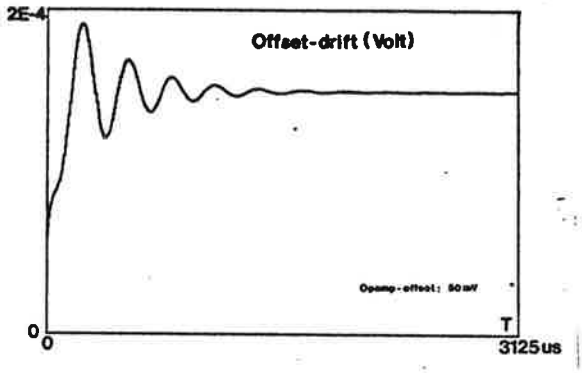


Fig 3

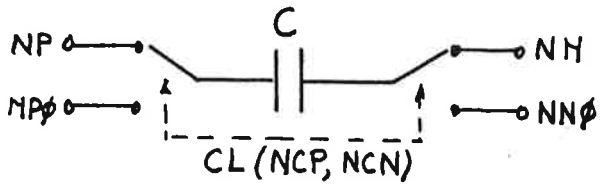
Fig. 2. and 3. illustrate an application of the .SCTIME mode to compute the impulse response of an elliptic SC filter aswell as the influence of an offset of 50 mV of the amplifiers used in this filter. We refer to [5] which also shows the application of the .SCTIME mode to study offset drift in an 8 phase filter as well as a study of the influence of nonlinear junction capacitance on drift of a SC integrator. Using the charge-sources it is also possible to study the effect of leakage currents on the operating point of SC filters. Notice that the value of the charge source at time t_k then needs to be found by integrating the leakage current i_1 over the previous time slot i.e.

$$q_{1,k} = i_1 \cdot \Delta_{k-1}$$

2.2.2. Top level .SCFREQ mode

Control statement : .SCFREQ NLIN= or NDEC= FSTART= FSTOP= (FSAMPLE=) &
(BAND=) (CONT) (SINC) (OUTSLOT=) (AMPL) (PHASE)

Allowed network elements : Idem as in the .SC TIME mode. Notice however that voltage and charge sources (not driving switches) cannot be time dependent. The value (VAL=) of a source is interpreted as the effective sinusoïdal value with zero phase. Furthermore it is possible to use an S4 switch defined as follows :



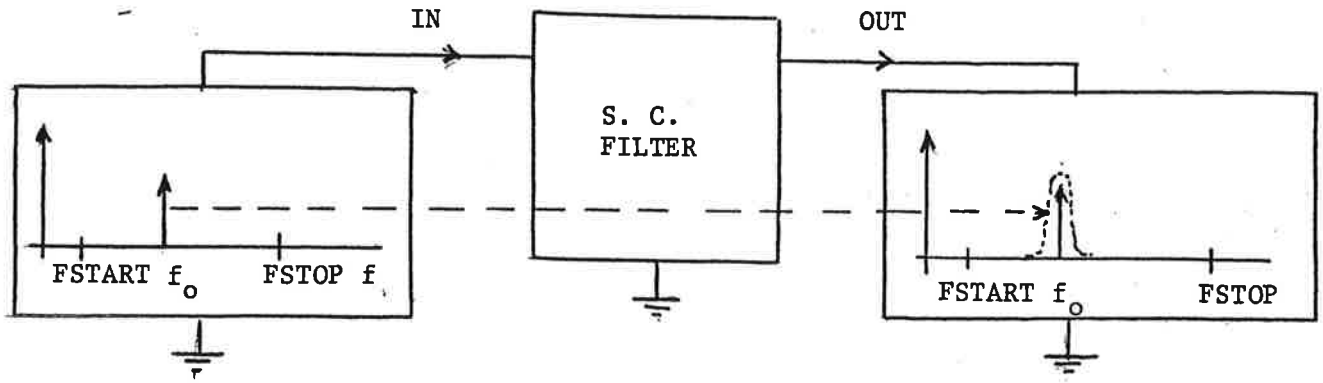
S4 ..... NP(=) NN(=) NPϕ(=) NNϕ(=) NCPC(=) NCN(=) C(=) VT(=)
The switches are in position (NP, NN) if (NCP)-V(NCN) ≥ VT. Otherwise it is in (NPϕ, NNϕ).

Type of analysis : For SC networks consisting of the above defined elements the frequency response of amplitude (AMPL) or phase (PHASE) or both (if no AMPL nor PHASE present) is calculated. The spectrum extends from FSTART to FSTOP and contains NLIN frequency points for a linear scale or NDEC frequency points / decade for a logaritmic scale.

In what follows the options BAND, CONT, SINC and OUTSLOT are discussed.

1. BAND OPTION :

The (BAND=) option allows for the study of aliasing (or folding) effects due to the time variant character of SC filters. If this card is omitted the computed response corresponds to the experimental set-up given in Fig. 4.



INPUT SOURCE
SWEEP GENERATOR
FSTART$\leq f_o \leq$FSTOP

TRACKING SELECTIVE
VOLTMETER MEASURING
OUTPUT AT SAME f_o AS
SWEEP GENERATOR

Default .SCFREQ operation - equivalent measurement set up if no (BAND=) specified.

Fig. 4

If BAND is specified it has the following meaning illustrated in Fig. 5.

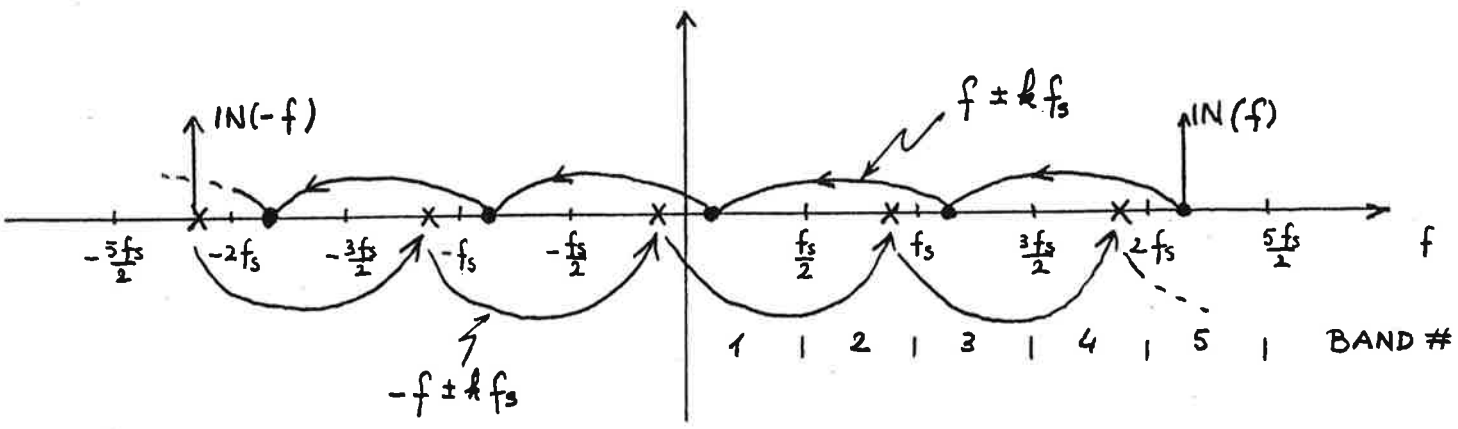


Fig. 5

Due to the time variant character of the SC circuit, aliasing and folding effects occur.

We define (see Fig. 5) :

BAND nr. n the frequency domain F_n such that $f \in F_n$ if :

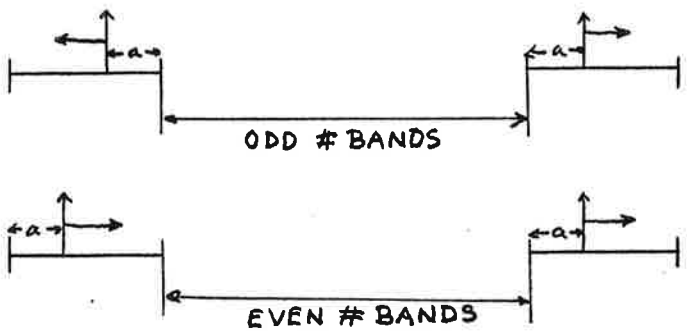
$$(n-1)\ \frac{f_s}{2} < f \leq n\ \frac{f_s}{2}$$

If within BAND=n (e.g. BAND=5 in Fig. 5) an input signal with frequency f is applied, a response can be expected for all $f \pm k\ f_s$ ($k \in \mathbb{Z}+$) (dots in Fig. 5). However, as f is a complex frequency, also a component with -f is present such that also responses are expected at $-f \pm k\ f_s$ ($k \in \mathbb{Z}+$) (crosses in Fig. 5). Fig. 5 shows that every frequency $f \in F_n$ causes one frequency response in every F_k (including itself but this corresponds to not specifying BAND=). The position of the response depends on the response band considered. If the response band is offset to the input band by an odd number of bands then it is a mirror image. On the other hand, if it is offset by an even number of bands then it is shifted by a multiple of f_s.

Now we are in a position to explain the (BAND=) option in DIANA.

BAND=value means that, at the INPUT of the filter, a sweep generator sweeps the input over BAND=value. The OUTPUT then is measured in the band specified by [FSTART, FSTOP] WHEREBY IT IS NECESSARY THAT FSTART & FSTOP BELONG TO A SINGLE BAND equal or different in value.*

The output is "observed" by a TRACKING selective voltmeter whereby tracking is to be understood in the sense of Fig. 5 and reillustrated below.



* This is not necessary if (BAND=) is not specified (set-up in Fig. 4).

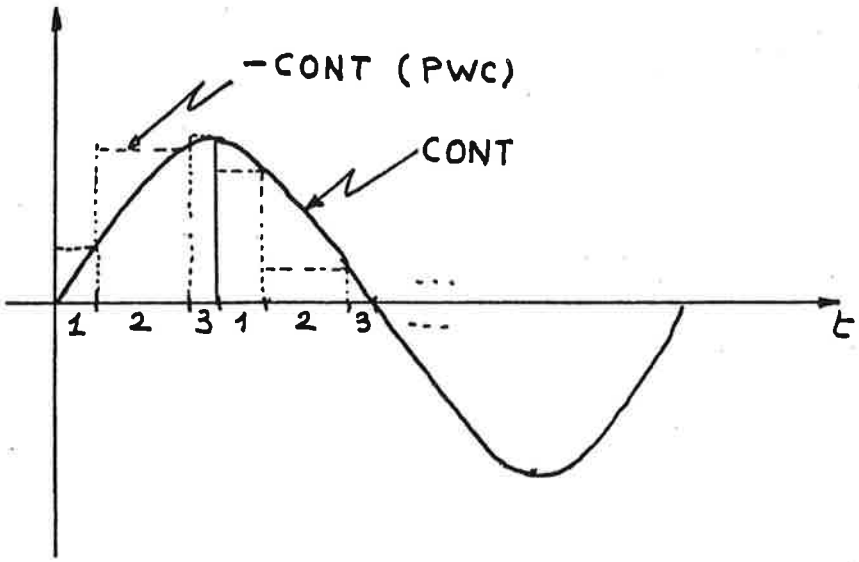


Fig. 6.a

2) (CONT) OPTION :

The CONT option relates to the effects caused by a potential electrical coupling, during at least one time slot, between the input source and the output node.

If indeed such a coupling exists it is necessary to consider the s.c. circuit as a mixture of a continuous and a time-discrete network. It has been shown in [8] that for that purpose an input wave form can be decomposed in a piecewise constant (PWC) input, sampled at the end of each time slot, and a remainder waveform which becomes zero at the end of each time slot.

The response of the s.c. network is a superposition of the response to the PWC input (difference equations) and the response to the remainder waveform as given by the equations (11) to (14) in [8]. When designing an s.c. filter it is common practice to do some handcalculations based on charge conservation and assuming a PWC input. One can then use z-transform techniques to derive the $H_{k\ell}(z)$ functions which then can be used to derive the frequency response for a PWC sinusoïdal input (eq. (13), [8]).

In such case the effects of a potential continuous coupling are neglected.

This situation can be simulated using the DIANA program when specifying :

-CONT

In that case the analysis proceeds as if the s.c. filter is driven by a PWC version of the input, sampled at the end of each time slot as illustrated in Fig. 6.a.

If CONT is specified or omitted the effect of the remainder waveform is included. This is the measured response if the input is a continuous time function.

For filters without a continuous I/O coupling both -CONT and CONT responses are the same.

3) SINC and OUTSLOT= OPTION :

The (SINC) and (OUTSLOT=) option have to do with the way the output of the SC filter is considered as illustrated in Fig. 6.b.

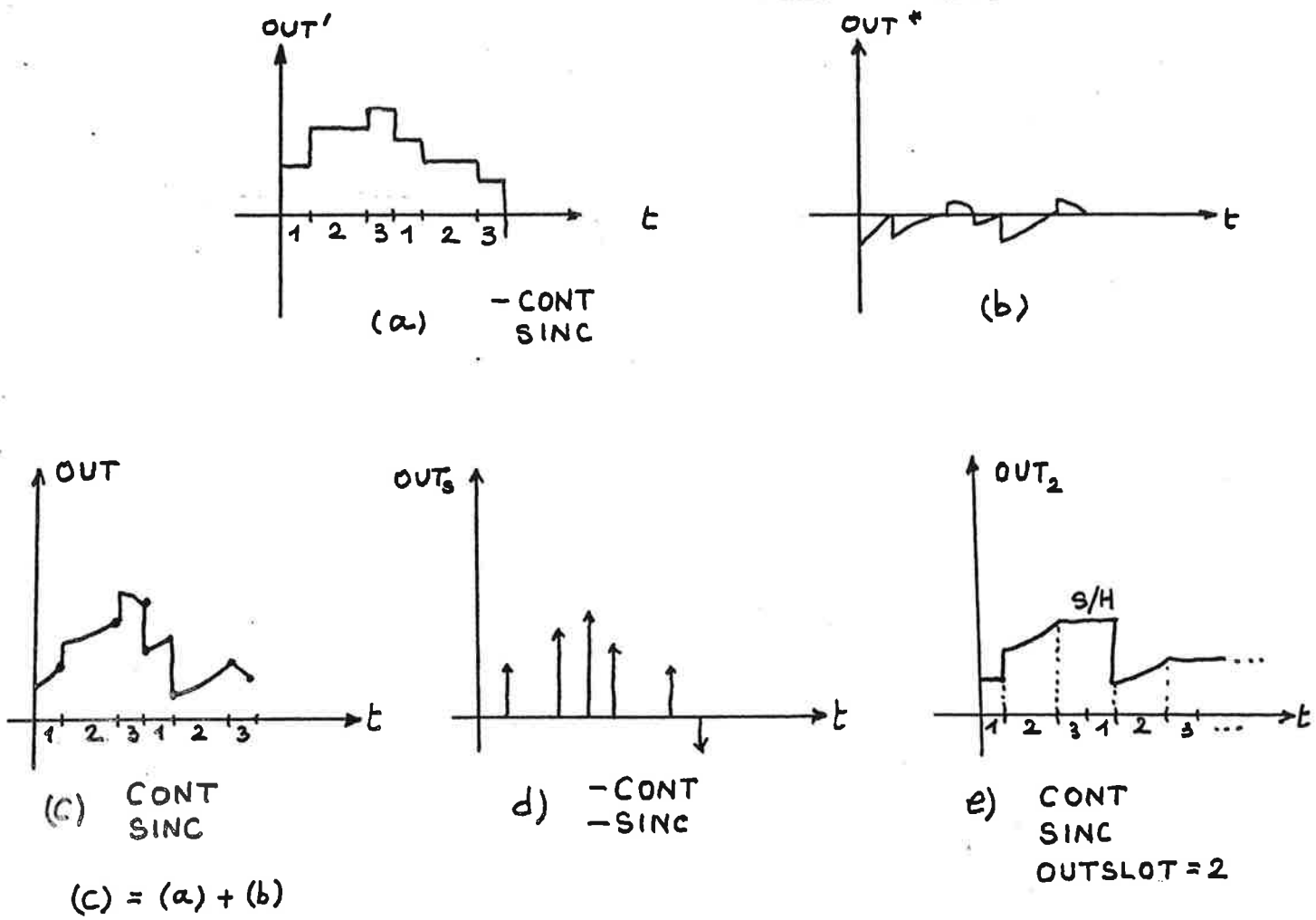


Fig. 6 b

The output of an s.c. filter can always be decomposed in the response to the PWC input (OUT') and the response to the remainder waveform (OUT*).

The word SINC refers to the

$$\alpha_k(\rho) = \mathrm{sinc}_k(\rho) \triangleq \frac{\sin \rho (t_{k+1}-t_k)/2}{\rho T/2} e^{j\rho(t_{k+1}-t_k)/2}$$

terms generated in the output response due to the sample and hold effects in the output waveform (see eqs. (13) and (14), ref. [8]).

As these effects are normally present, SINC is optional. Only if :

-SINC

is specified (which only makes sense if also -CONT is specified (see Fig. 6.b(d)) all the sample and hold effects are neglected and it is as if the output consists of a train of δ-functions i.e. all

$$\alpha_k(\rho) = 1$$

in eq. (13) [8].

If OUTSLOT= is not specified, it is assumed that the output waveform is observed during all timeslots.

In many circuits however the output is only observed (sampled) during one or more time slots while it is being held during the others.

Fig. 6b(e) illustrates the case OUTSLOT=2. Obviously OUTSLOT= can have more time slots specified. It should also be clear that OUTSLOT= value is not compatible with the -SINC option.

The above defined possibilities are illustrated by the following example which is a simple pole-zero realization with continuous I/O coupling.

4) Example for TOP .SCFREQ analysis :

Fig. 7 illustrates a simple pole-zero filter configuration and two clocking shemes, A and B.

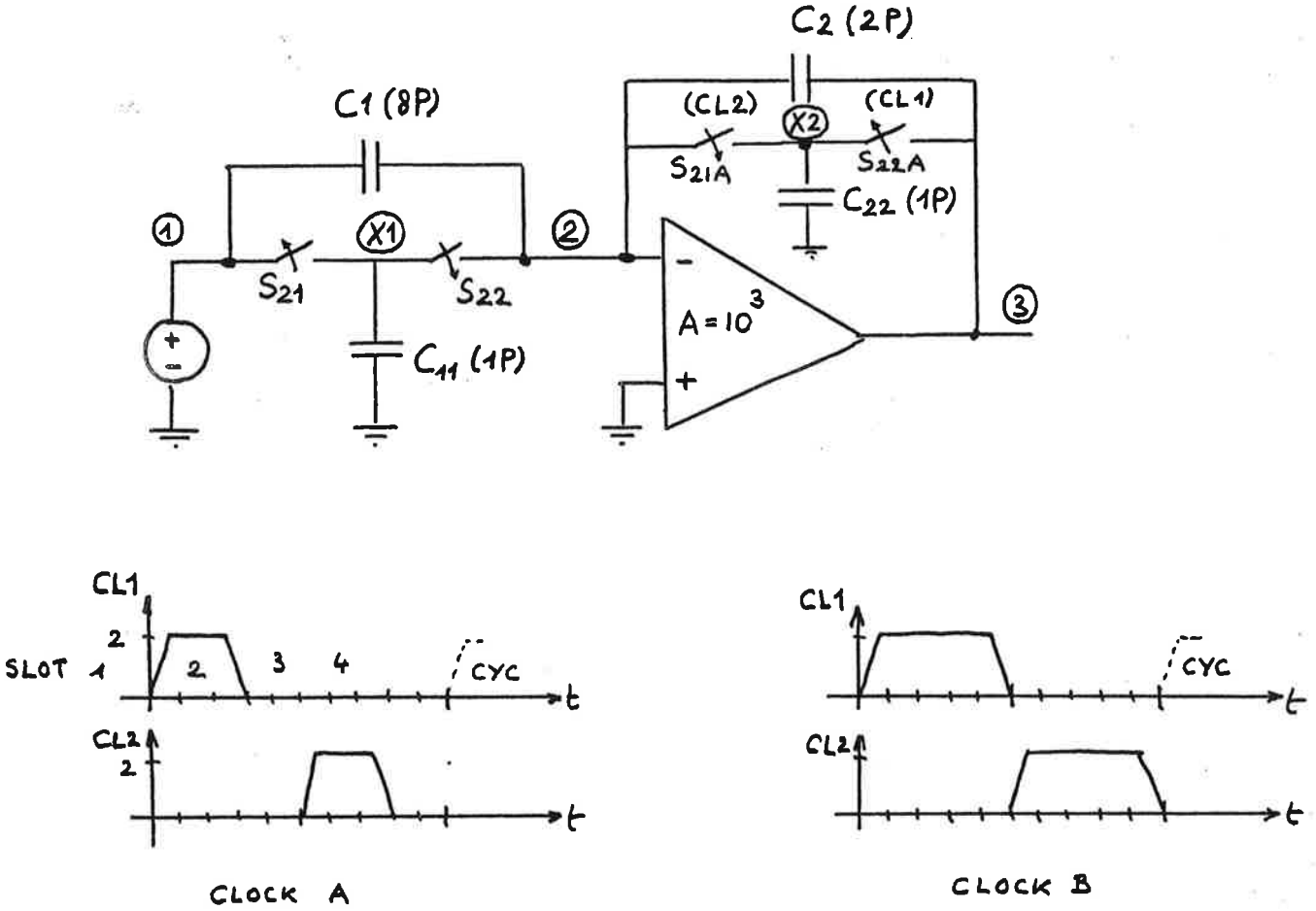


Fig. 7

Notice that for clock scheme A all duty cycles are equal to 25 %. A simplified analysis using "equivalent resistors" shows that to a first approximation :

$$H(jf) \approx - \frac{1 + j\frac{f}{f_z}}{1 + j\frac{f}{f_p}}$$

with : $f_z = \frac{1}{16\pi T} = 1{,}99$ kHz

and $f_p = \frac{1}{4\pi T} = 7{,}96$ kHz

In between these frequencies we have a + 20 dB/decade response with a 12 dB amplification for high frequencies.

We will now consider and compare a number of alternative runs to illustrate most of the options.

RUN 1. Using -CONT, -SINC and linear freq. scale, clock scheme A :

```
**********************************************************************

 ESAT     TREBLE TONE CONTROL FILTER

**********************************************************************

 .SCFREQ NLIN=1000 FSTART=0HZ FSTOP=1MEGHZ FSAMPLE=100KHZ -CONT -SINC
 .OPTIONS -OUT
 INPUT CL1 V-T=0 0 2 0.5U 2 2.5U 0 3U 0 10U CYC
 INPUT CL2 V-T=0 0 0 5U 2 5.5U 2 7.5U 0 8U 0 10U CYC
 PRINT 3
 VIN 1 0 1
 S21 1 X1 CL1 0 VT=1
 S22 2 X1 CL2 0 VT=1
 S21A 2 X2 CL2 0 VT=1
 S22A 3 X2 CL1 0 VT=1
 C11 X1 0 1P
 C22 X2 0 1P
 C1 1 2 8P
 C2 2 3 2P
 XV1 3 0 0 2 1K
 .END
```

RUNTIME : 10 SEC

FIG 8

Fig. 8 shows the input description.

Fig. 9 shows the amplitude plot of the output node ③ on a linear scale. Notice that, due to the 4 equal time slots the apparent sampling frequency is 4 times the basic 100 kHz sampling frequency.

Since we use a -CONT, -SINC option the spectrum is folded at 200 kHz and 600 kHz. The baseband response is periodic with a period of 400 kHz.

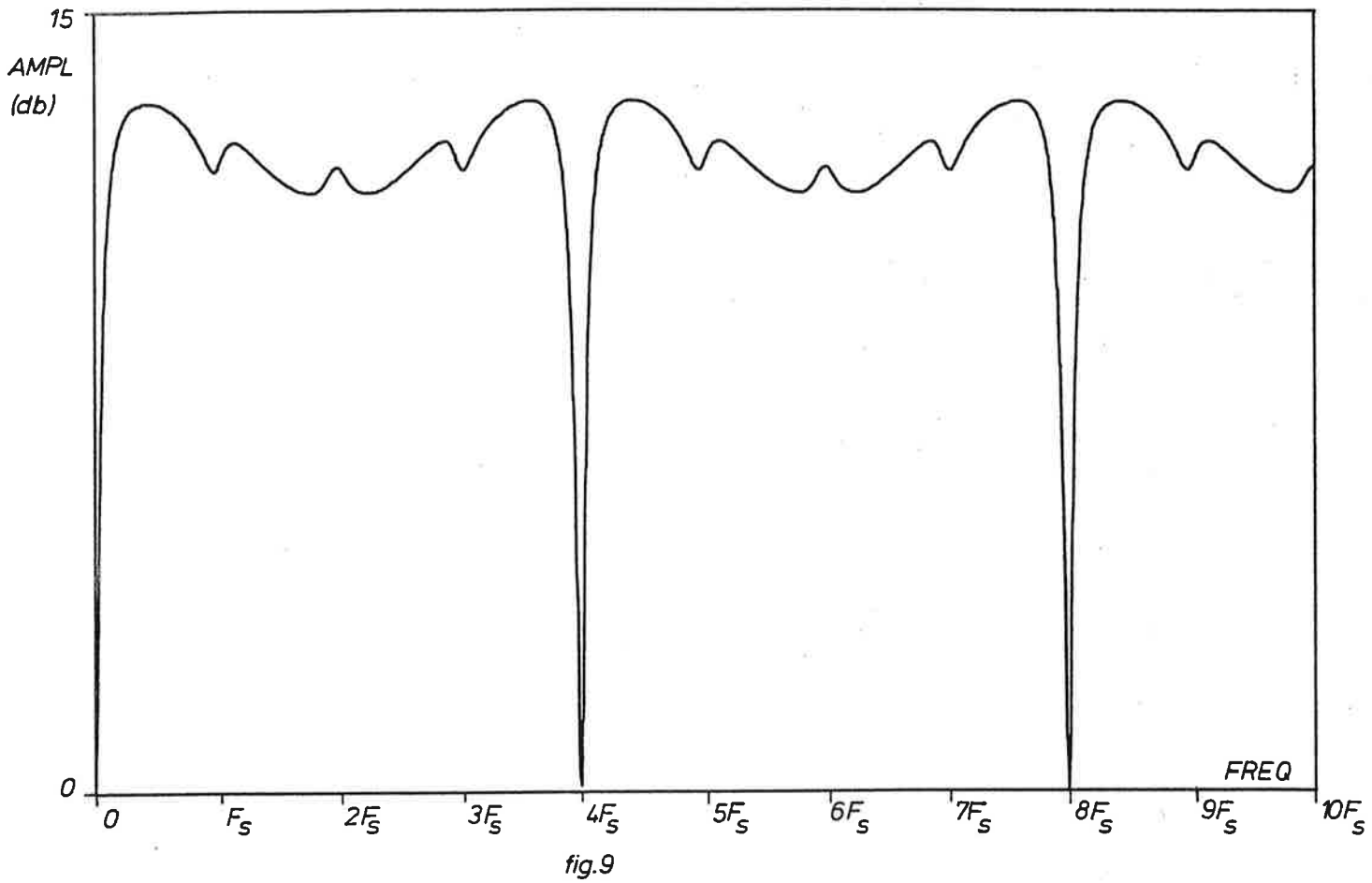


Fig. 9

RUN 2. Using -CONT, (SINC), lin. freq. scale, clock scheme A :

Same input as RUN 1 except for .SCFREQ card shown below.

```
.SCFREQ NLIN=1000 FSTART=0HZ FSTOP=1MEGHZ FSAMPLE=100KHZ -CONT
```

The output plot is shown in Fig. 10.

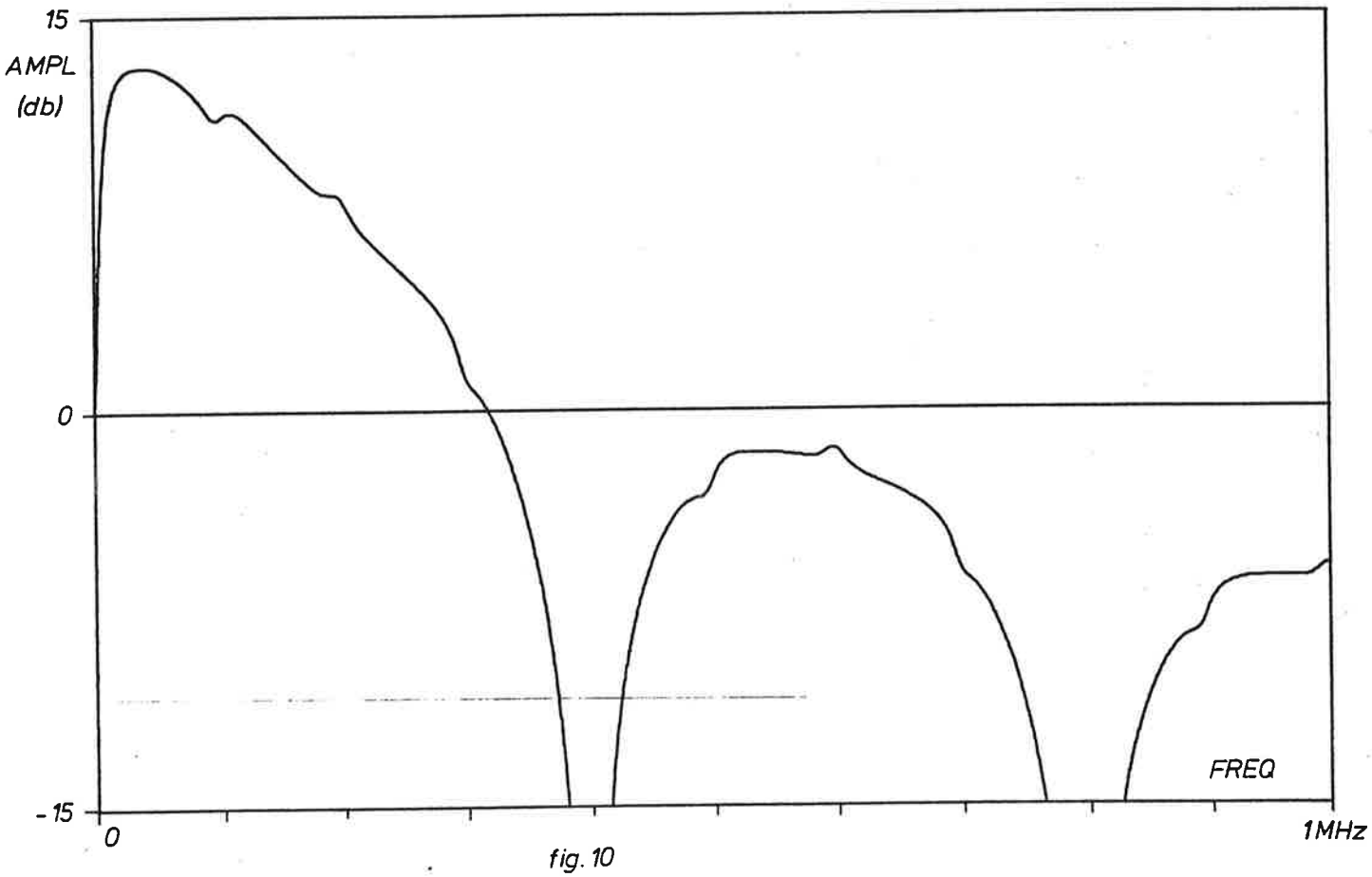


fig. 10

Since now the output is held each time over each 25 % duty cycle we will get the same response as earlier but now it will contain sinc effects at 4 times the basic sampling frequency since :

$$t_{k+1} - t_k = \frac{1}{4} T$$

for k = 1 to 5.

RUN 3. Using (CONT) (SINC), log. freq. scale, clock scheme A :

Same input as RUN 1 except for .SCFREQ which becomes :

```
.SCFREQ NDEC=250 FSTART=100HZ FSTOP=1MEGHZ FSAMPLE=100KHZ
```

The output plot with logarithmic frequency scale is shown in Fig. 11, curve A.

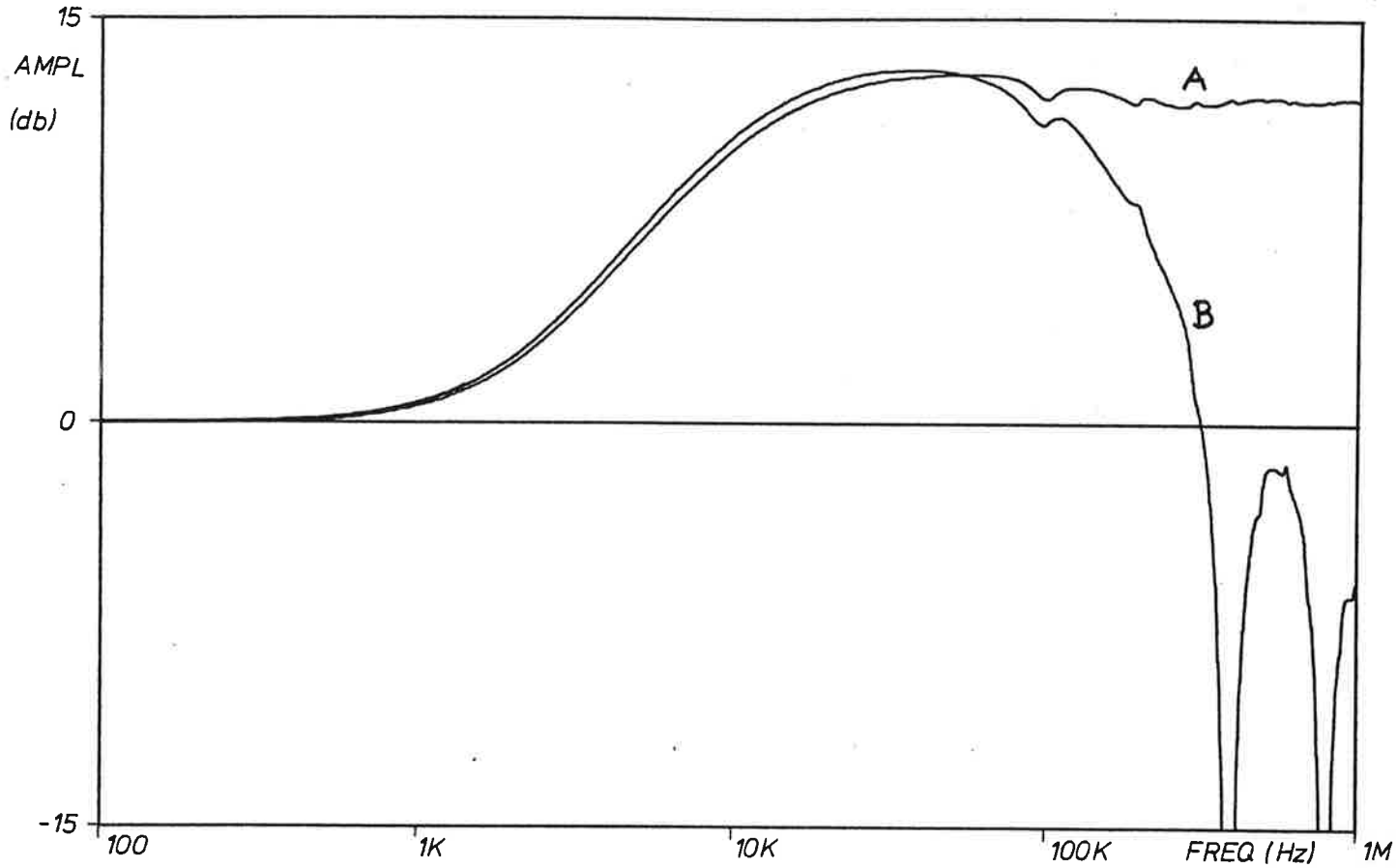


fig. 11

When comparing the result with the -CONT, SINC option given by curve B we see that the zero's at 400 kHz and 800 kHz have disappeared as a result of the fact that at these frequencies the continuous I/O coupling due to C1 and C2 still provides a 12 dB gain which is not affected by the sinc effects causing the zero's.

RUN 4. Effects of OUTSLOT= option :

RUN 4.a : -CONT, (SINC), OUTSLOT=2, lin. freq. scale.

In this case we consider a PWC input as in RUN 2 but the output is sampled during time slot 2 (when CL1 is true) and held over the three other time slots.

In this case the output signal is constant over the 4 time slots of the clock cycle and therefore the sinc effects have a period of 100 kHz which is clearly visible in Fig. 12.

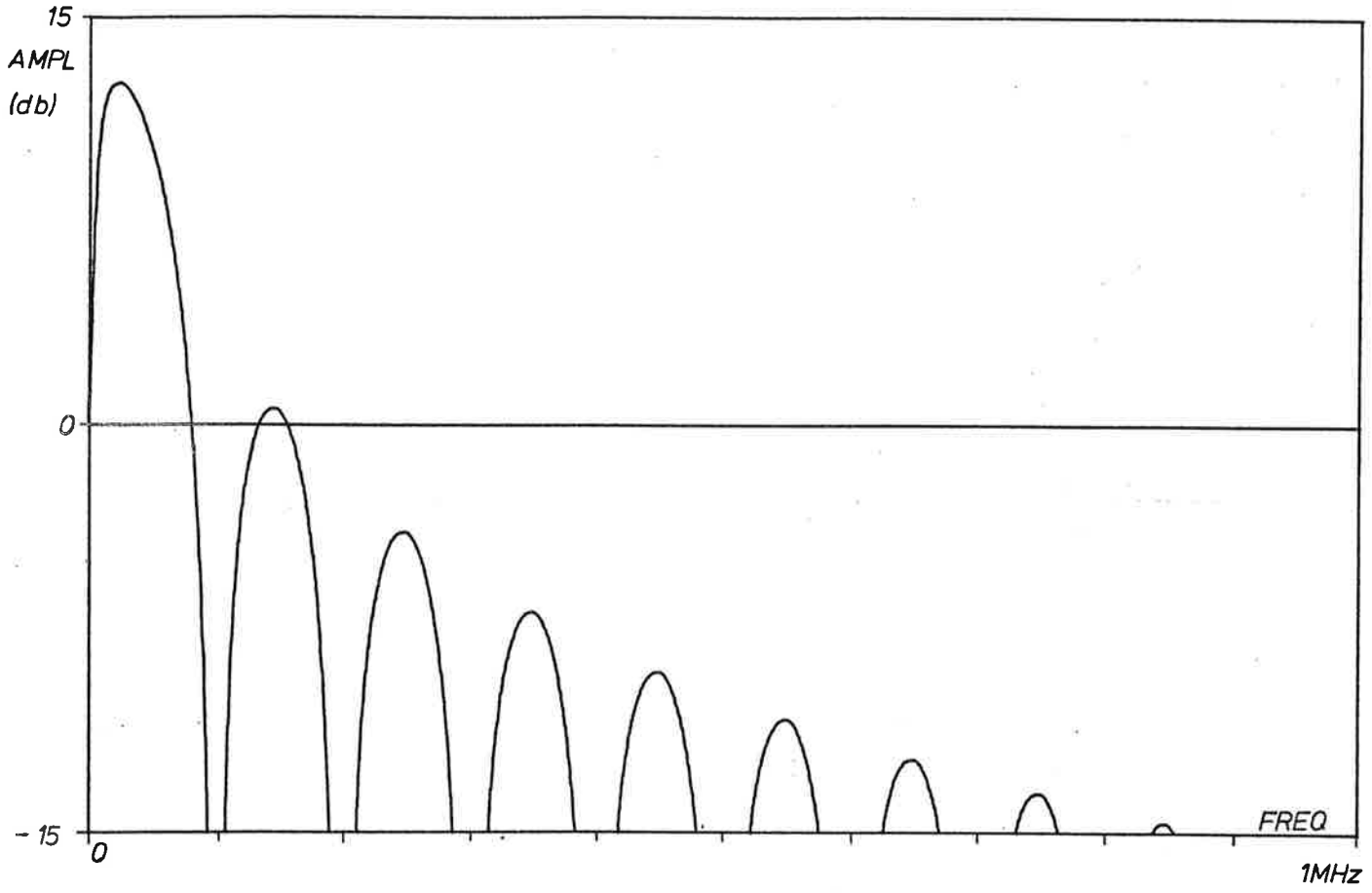


Fig. 12

RUN 4.b : (CONT), (SINC), OUTSLOT=2, linear freq. scale :

In this case the input is continuous such that in the time domain, during time slot 2 a continuous feedthrough of the input occurs during 25 % of the clock-cycle whereas the value at the end of this interval is held over 75 % of the remainder of the clock-cycle.

As a result two effects occur :

a) the sinc effects in Fig. 12 are attenuated by the continuous effects through C1, C2.
b) the S/H effects occur during resp. 25 % and 75 % of the duty cycle such that the minima of the sinc effects are no longer occurring at multiples of 100 kHz but of 400/3 = 133,33 kHz.

These results are shown in Fig. 13.

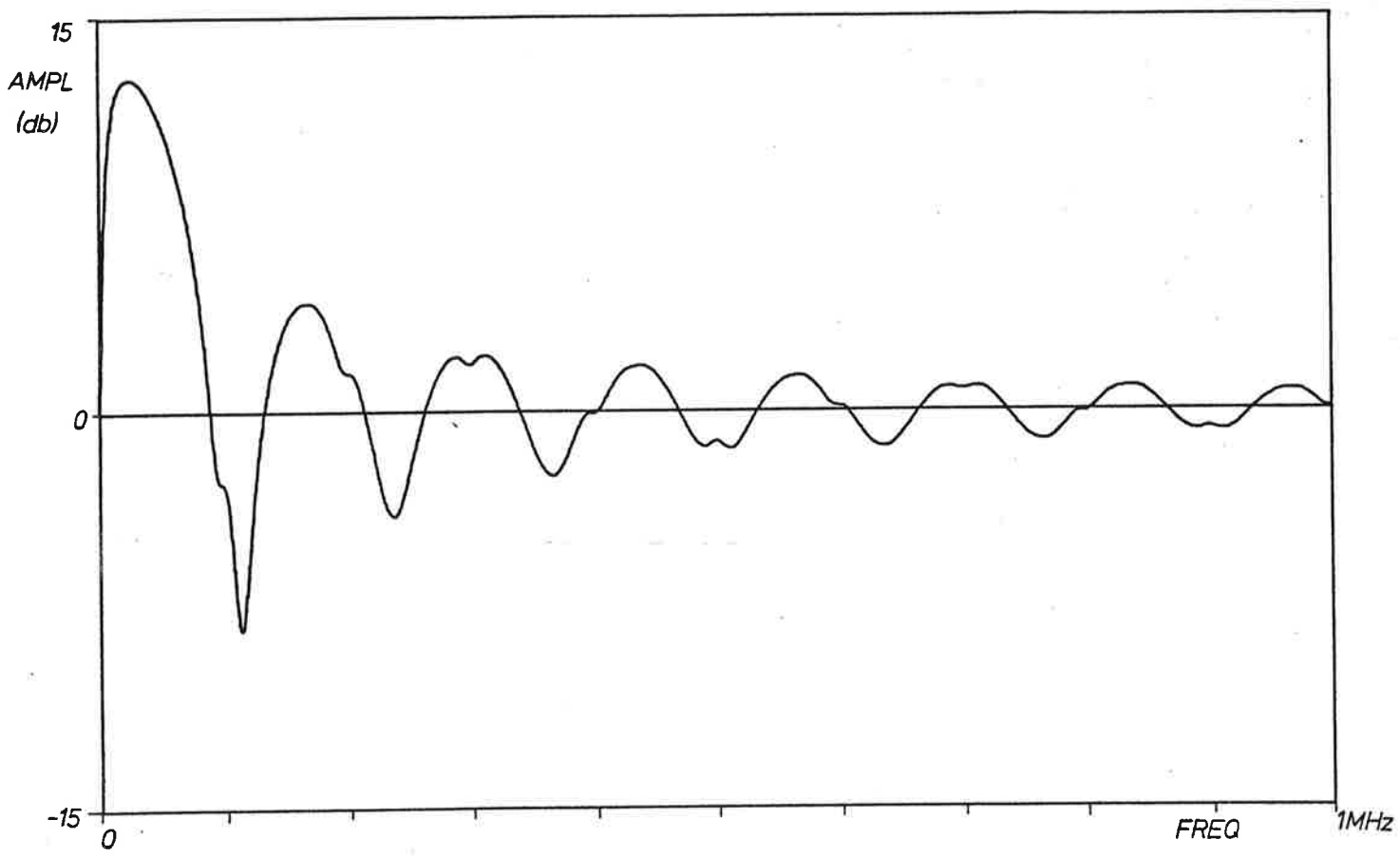


Fig. 13

RUN 5. Effect of clock duty cycle :

Fig. 14 shows a rerun of the case CONT, SINC but now with clock scheme B instead of A (curve B). For reference, curve A gives the same result with clock scheme A.

In this case an effect of the duty cycle of the clock is clearly visible. This effect occurs because of the continuous coupling since the different $H_{k\ell}(e^{j\omega t})$ are nonzero and are to be added with different phase factors.

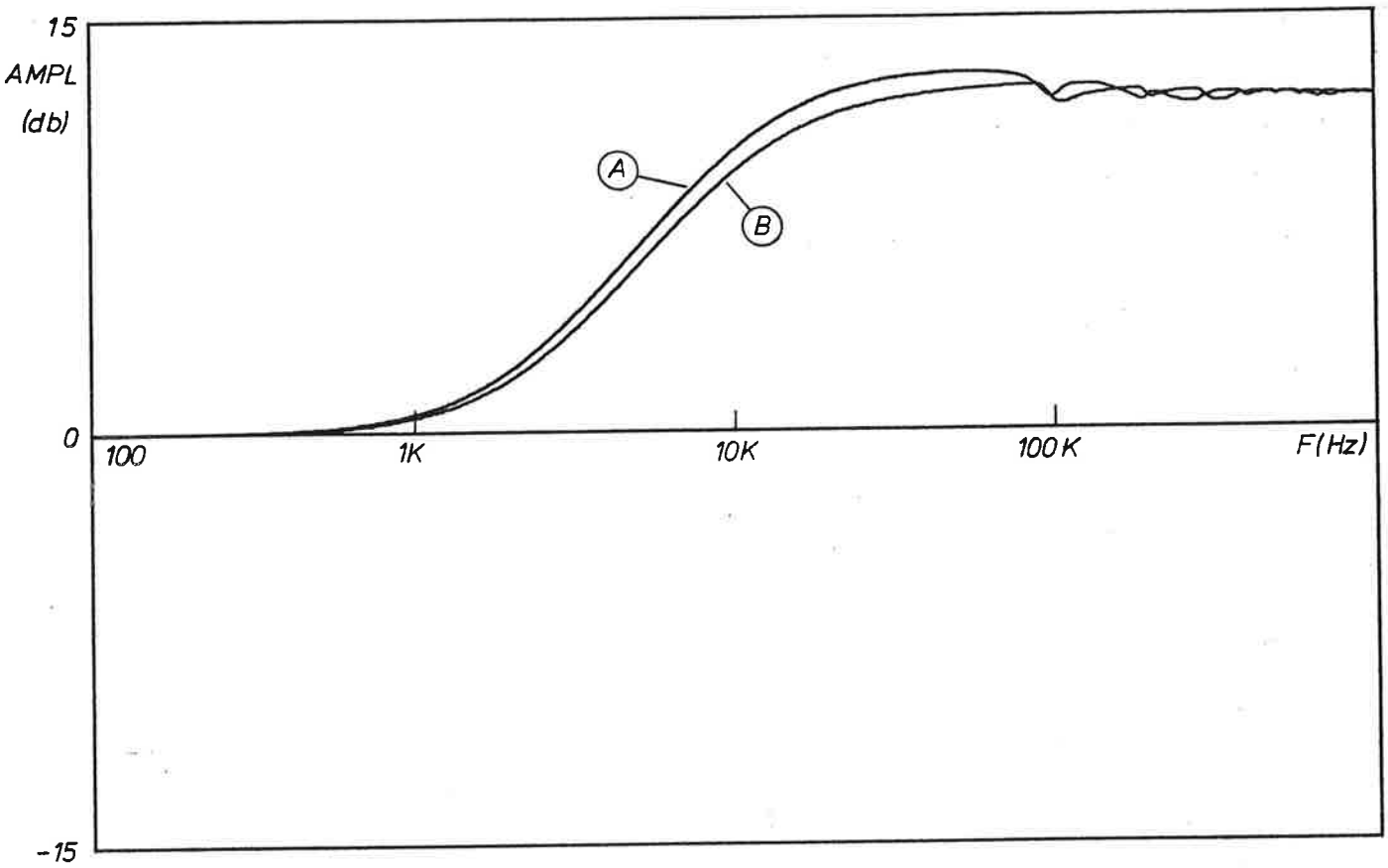


Fig. 14

RUN 6. Effect of aliasing : (BAND=) option :

Shown below is the input to describe the aliasing effect occuring by scanning band 3 (BAND=3) i.e. the input changes from 100 kHz to 150 kHz. The output is observed from 100 Hz to 50 kHz which belongs to BAND=1. The offset of the bands is even such that sweeping occurs parallel (e.g. input at 102 kHz causes response at 2 kHz). The run is done including CONT and SINC effects.

The sensitivity to a node (k) is defined as the amplitude and phase sensitivity of output node (out) to a fictitious capacitor C_k of zero value from node (k) to ground i.e.

$$S_k^{out} = \frac{\partial (20 \log_{10} |V_{out}|)}{\partial C_k} \qquad \text{(dB/pF)}$$

and

$$S_k^{(out)} = \frac{\varphi(out)}{\partial C_k} \qquad \text{(degrees/pF)}$$

These sensitivities allows the designer to quickly estimate the influence of parasitic stray capacitance added to the node (k). Notice that sensitivities are computed for the full frequency spectrum (FSTART, FSTOP) defined in the .SCFREQ card and only for the SINC and CONT option. -SINC and -CONT options are overwritten.

Examples :

Shown below is the input deck for the circuit defined in Fig. 6 where sensitivities with respect to capacitances C1, C11, C2, C22 and node X1 are requested. The output plot of this run is shown in Fig. 17.

```
**********************************************************************
*
*         ESAT     TREBLE TONE CONTROL FILTER
*
**********************************************************************
        .SENS CAP=C11 C22 C1 C2 NODE=X1
        .SCFREQ NDEC=250 FSTART=100HZ FSTOP=1MEGHZ FSAMPLE=100KHZ
        .OPTIONS -OUT
        INPUT CL1 V-T=0 0 2 0.5U 2 2.5U 0 3U 0 10U CYC
        INPUT CL2 V-T=0 0 0 5U 2 5.5U 2 7.5U 0 8U 0 10U CYC
        PRINT 3
        VIN 1 0 1
        S21 1 X1 CL1 0 VT=1
        S22 2 X1 CL2 0 VT=1
        S21A 2 X2 CL2 0 VT=1
        S22A 3 X2 CL1 0 VT=1
        C11 X1 0 1P
        C22 X2 0 1P
        C1 1 2 8P
        C2 2 3 2P
        XV1 3 0 0 2 1K
        .END
```

This example clearly shows many of the possibilities of analysis of s.c. networks in the frequency domain of ideal linear s.c. networks using the .SCFREQ mode at TOP-level simulation.

The last mode of TOP-level simulation is the .SENS mode allowing for the calculation of sensitivities using the adjoint network concept. For a detailed discussion on this concept see [7].

2.2.3. The .SENS option

The .SENS option allows for the computation of sensitivities of amplitude and phase to :
- capacitor values
- gain of op-amps
- "nodes"

This option is very useful for :
- optimization
- tolerance influence
- estimate of influence of stray capacitance

The allowed network elements are the same as for the .SCFREQ mode. To obtain sensitivities it is sufficient to add the following control card :

.SENS CAP = list of capacitor names; VDV = list of VDV names ; NODE = list of node names

When this card is added, the amplitude and phase sensitivities of the first output node specified in the print card are computed.

The sensitivities are defined as follows :

- capacitance value sensitivity :

$$S_c^{V_o} = \frac{\partial(20 \log_{10}|V_o|)}{100\,\partial C/C} \qquad \text{(dB/\% capacitor value)}$$

$$S_c^{\varphi(V_o)} = \frac{\partial \varphi}{100\,\partial C/C} \qquad \text{(degrees/\% capacitor value)}$$

- op-amp gain sensitivity :

Idem but C=A (op-amps gain factor).

Of particular interest is the "node" sensitivity defined as follows :

2.3. INTERMEDIATE level analysis :

Intermediate level analysis refers to S.C. networks including resitive (i.e. time constant) effects. All switches in S.C. networks are MOS transistors and hence have a finite channel resistance in the on state. Op-amps have poles in their transfer function even as finite output resistance. Furthermore all these resistors and operational amplifiers have noise sources.

These effects can have a serious influence e.g. on high Q filters or on filters operating at high sampling rates. They are essential for a prediction of the noise behavior of S.C. networks.

Referring to table 1, three different modes of operation at INTERMEDIATE level are possible :

.SCFREQ
.NOISE
.TRAN

2.3.1. The .SCFREQ option at INTERMEDIATE level :

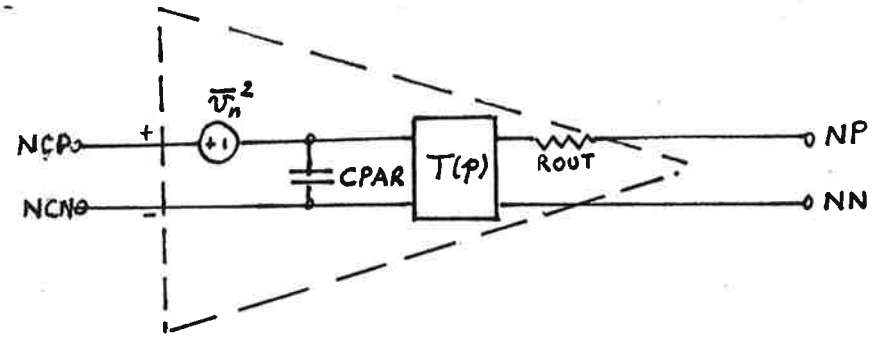
Control card : .SCFREQ NLIN= or NDEC= FSTART FSTOP (FSAMPLE=) (BAND=)

Allowed network elements :

In addition to capacitors also resistors and S2 switches with finite on resistance are allowed i.e.

S2 .... NP NN NCP NCN R= VT=

No S3 and S4 switches are allowed in the actual version of the program. Furthermore, in addition to the usual voltage and current sources, also the four dependent sources mentioned on p. 7 are allowed but in addition to them also an operational amplifier model can be specified as shown in Fig. 18.



OPA ..... NP NN NCP NCN GAIN(=) ROUT(=) CPAR(=) POLE(=) WØ(=) Q(=)
WHITE NOISE(=) 1/F-BREAK(=)

Fig. 18

This model realizes the following internal transfer function :

$$T(p) = GAIN/(1+p/2\pi.POLE)(p^2+2p\ W\emptyset/Q + W\emptyset^2(1+Q^{-2}))$$

i.e. it has a negative real pole and a complex conjugate pole-pair.

In addition it has an input capacitance CPAR and an output resistance ROUT. Also noise sources can be specified in the NCP input lead.

The WHITE NOISE(=) refers to a frequency independent noise source value expressed in Volts/$\sqrt{HZ}$ whereas 1/F-BREAK(=) refers to the frequency at which 1/f noise voltage is equal to the white noise voltage specified by the WHITE NOISE(=) card. For the time being this value is used to compute noise transfer functions as to be discussed below.

Of course it is also possible for the user to construct his (her) own linear op-amp model using C,R and dependent sources.

Type of analysis :

Notice that basically the presence of a resistive element in the circuit description will automatically invoke the INTERMEDIATE level type of analysis. This analysis is based on reference [6].

It should hereby be noticed that the method given in [6] implies that the S.C. network can have transient effects within all timeslots but it is still necessary that the S.C. network reaches a steady state at the end of each timeslot.

Whether such condition is satisfied can be analyzed by a .TRAN type analysis (see further). In future versions also the case in which no steady state is reached will be implemented.

Example :

As an example Fig. 19 shows the input deck for the analysis of the circuit used in the previous examples (Fig. 16) in INTERMEDIATE level.

```
ESAT    TREBLE TONE CONTROL FILTER
.OPTIONS STORE
.SCFREQ NDEC=100 FSTART=100 FSTOP=1MEG BAND=0
INPUT CL1 V-T=0 0 2 0.5U 2 2.5U 0 3U 0 10U CYC
INPUT CL2 V-T=0 0 0 5U 2 5.5U 2 7.5U 0 8U 0 10U CYC
PRINT 3
VIN 1 0 1
S211 1 X1 CL1 0 R=10K VT=1
S212 2 X1 CL2 0 R=10K VT=1
S221 2 X2 CL2 0 R=10K VT=1
S222 3 X2 CL1 0 R=10K VT=1
C11 X1 0 1P
C22 X2 0 1P
C1 1 2 8P
C2 2 3 2P
OPA1 3 0 0 2 POLE=1K GAIN=1K ROUT=10K CPAR=0.5P
.END
```

Fig. 19

Notice now that all switches have an on resistance of 10 KΩ. Furthermore the above mentioned op-amp model (OPA1) with a pole of 1 kHz, an output impedance of 10 KΩ and an input capacitance of 0.5 pF is used.

Fig. 20 shows the computed response (curve b). It is compared also with the response computed in TOP level mode (curve a).

The -20 dB decade fall of the spectrum for frequencies above 100 kHz results from the pole of the operational amplifier but it is also clear that even in the baseband ($f \lesssim 50$ kHz) there is a deviation between the TOP and INTERMEDIATE level analysis. This effect can be traced back to phase shift in the op-amp due to the pole at 1 kHz.

This effect of phase shift can cause negative resistance effects in integrators and can lead to peaking in ladder filters.

Fig. 21. shows the computed response in the passband for the elliptic filter shown in Fig. 2.. The top curve in Fig. 21 is obtained from an ideal op-amp with gain of 10^6. The bottom curves are for a gain of 10^3 and three different unity gain bandwidths. The effect of peaking is clearly visible.

2.3.2. NOISE transfer function calculations :

When resistive effects and frequency response of op-amps are included as in the INTERMEDIATE level it becomes possible to perform noise calculations if the thermal noise of resistors and op-amps is included.

Noise calculations in S.C. filters are complicated by the fact that, due to aliasing effects, noise is folded back into the frequency range of interest, so the noise transfer functions from all noise sources to the output node need to be computed and this from all frequency BANDS back to the BAND under consideration. These results then have to be added quadratically.

This calculation can be simplified considerably by using the adjoint network concept as discussed in [7]. This option is at present being implemented into DIANA.

For the time being it is however possible, using the .SCFREQ option, to compute all noise transfer functions by adding the noise sources and then performing calculations over all frequency bands using the BAND= option.

An example is given in Fig. 22 which is the input to compute the noise transfer function of switch S211 from BAND=2 to the baseband for the example circuit used in this paper. Notice the noise source E=1 is S211.

```
ESAT    TREBLE TONE CONTROL FILTER
.OPTIONS STORE
.SCFREQ NDEC=20 FSTART=100 FSTOP=50K BAND=2
INPUT CL1 V-T=0 0 2 0.5U 2 2.5U 0 3U 0 10U CYC
INPUT CL2 V-T=0 0 0 5U 2 5.5U 2 7.5U 0 8U 0 10U CYC
PRINT 3
VIN 1 0 0
S211 1 X1 CL1 0 R=10K E=1 VT=1
S212 2 X1 CL2 0 R=10K VT=1
S221 2 X2 CL2 0 R=10K VT=1
S222 3 X2 CL1 0 R=10K VT=1
C11 X1 0 1P
C22 X2 0 1P
C1 1 2 8P
C2 2 3 2P
OPA1 3 0 0 2 POLE=1K GAIN=1K ROUT=10K CPAR=0.5P
.END
```

Fig. 22

Fig. 23 shows results of such calculations for the two switches S211 and S212 as well as for the noise source of the op-amp and this for a number of different bands to baseband. Notice that the transfer functions for the two input switches differ considerably for lower band to band interactions. This effect results from the effect of the continuous coupling, which is present in both clock phases for S211 but for S212 only during phase 2.

For the op-amp continuous coupling is present during both clock phases. Notice that continuous coupling effects have an advantageous effect on noise behavior as folding effects are attenuated by it.

2.3.3. TRAN option at INTERMEDIATE and DOWN level :

Simulation of S.C. filters including resistors and even MOS transistor models or logic and timing macromodels in the time domain is possible if the TRANSIENT analysis mode .TRAN of DIANA is used. In such case the program performs a full transient analysis of the circuit under consideration.

It is of course necessary, in such case, to use a timestep DELTA which is small enough to see transient details for timeslot e.g. 5 ... 10 points/time slot.

Such type of analysis is expensive but can be very useful to study in detail e.g. the following problems :

- DC stability (offset and drift effects).
- Clock-feedthrough effects due to switch parasitic capacitances.
- Study of switching behavior of operational amplifiers described at the transistor level.
- Derivation of model parameters for INTERMEDIATE level simulation by op-amps simulation at the DOWN level (using transistor models).
- Verification of digital steering logic for adaptive S.C. filters or for A/D and D/A converters.

  etc.

For a description on how to use DIANA for these applications one refers to a detailed manual of the program [3].

The following is an example of how the program can be used to study clock-feedthrough effects. Fig. 24 shows a simulation of the elliptical filter shown in Fig. 2 of this text. The input voltage is zero but all switches have been substituted by MOS transistor models available in the CIRCUIT (DOWN) mode of DIANA. Furthermore the op-amps are described by a model with a single pole at 4,5 kHz and a gain of 10^3. Clock frequency is 128 kHz with a swing of -5V to +5V as shown in the upper plot in Fig. 24.

Now clock-feedthrough occurs through the MOS Cg and Cgd capacitors. These effects are shown at node (7) (See Fig. 2), the virtual ground of op-amps XVE and output node (10).

One can clearly see that clockfeedthrough causes an output DC offset of 0.35 Volts. The spikes at the input of the op-amp result from instantaneous voltage division when the MOS transistors are switched on as well as from the finite bandwidth of the op-amps. This simulation over 1000 time points takes 3 minutes, 30 sec. on a VAX 11/780 under VMS operation system.

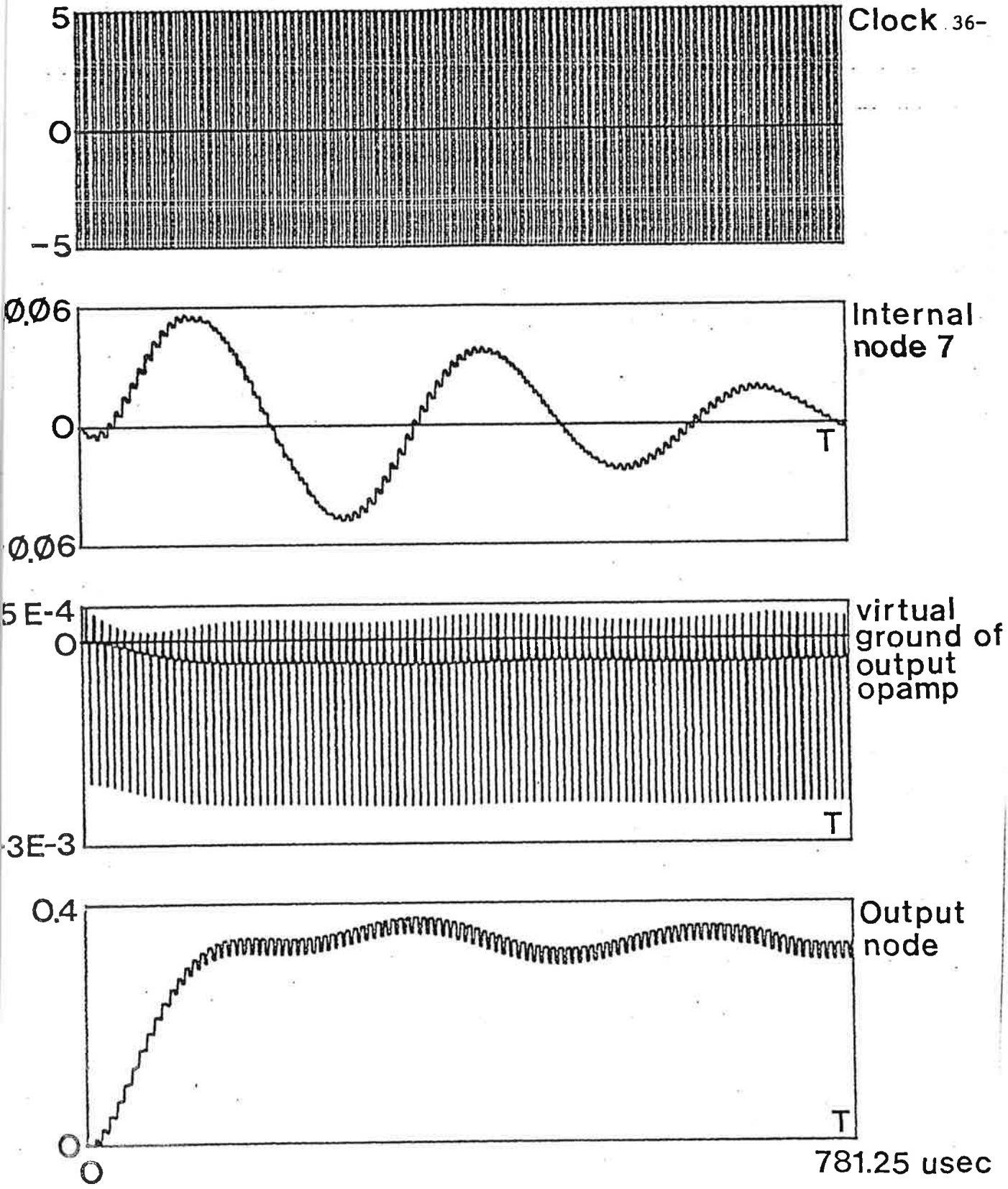


Fig. 24

3. Conclusion :

It has been shown how the DIANA program can be used as a general top-down design tool for switched capacitor networks. No limitations to the number of clock-phases or to the network elements are imposed. In the future the NOISE option will be completed such that direct noise computation will be possible. Also the restriction to obtain a final steady state in the case of resistive S.C. networks will be eliminated.

References :

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[2] H. De Man, J. Rabaey, G. Arnout, J. Vandewalle : "DIANA as a Mixed-Mode Simulator for MOSLSI Sampled Data Circuits", Proc. IEEE Int. Symp. on Circuits and Systems, 1980, pp. 435-438, June 1980.

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[6] J. Rabaey, J. Vandewalle, H. De Man : "On the analysis of switched capacitor filters in the frequency domain, including all parasitics", Proc. IEEE Symp. on Circuits and Systems, Chicago, April 1981, pp. 868-871.

[7] J. Vandewalle, H. De Man, J. Rabaey, "The adjoint switched capacitor network and its application to frequency, noise and sensitivity analysis", Circuit Theory and Applications, Vol. 9, pp. 77-81, 1981.

[8] J. Vandewalle, H. De Man, J. Rabaey, "Time, frequency and z-domain Modified Nodal Analysis of Switched-Capacitor Networks", IEEE Trans. on Circuits and Systems, Vol. CAS-28, pp. 186-195, March 1981.