Reducing Circuit Soft Error Rate (SER): From Combinational to Sequential Circuits

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Due to current technology scaling trends such as shrinking feature sizes and decreasing supply voltages, nanoscale integrated circuits are becoming increasingly sensitive to radiation-induced transient faults (soft errors). Logical masking, electrical masking, and latching-window masking, which prevent transient events in logic circuits from being latched into memory elements, are weakened with continuous scaling trends. Therefore, soft errors, which have been a great concern in memories, are now a main factor in reliability degradation of logic circuits. A predictive model [1] showed that, unless explicitly dealt with, the SER of logic is expected to be comparable to that of unprotected memories.

In this session, I will introduce three approaches for soft error rate (SER) reduction. The first one [2], based on *redundancy addition and removal* (RAR), estimates the effects of redundancy manipulations and accepts only those with positive impact on circuit SER. Several metrics and constraints are proposed to guide the RAR algorithm toward SER reduction in an efficient manner. The second approach [3], based on *selective voltage scaling* (SVS), assigns a higher supply voltage to gates that have large error impact and contribute most to the overall SER. The number of gates operating at the higher voltage level, positively correlated with the power overhead, can be bounded by the appropriate use of level converters. The third approach [4], based on *clock skew scheduling* (CSS), adjusts the arrival times of clock signals to memory elements (latches or flip-flops) such that the probability of capturing unwanted transient pulses is decreased, as a result of more latching-window masking.

These three techniques (RAR, SVS, and CSS) target different parts of logic circuits. Given a logic circuit, the RAR-based approach focuses on restructuring its combinational block, while the approaches using SVS and CSS involve modifications on the power distribution and clock network, respectively. All of these proposed approaches, when integrated and applied in a particular order (*i.e.*, RAR → SVS → CSS), can thus provide additive improvements in SER.

REFERENCES

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