Compiler Frameworks for Leakage Power Reduction *

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Power leakage constitutes an increasing fraction of the total power consumption in modern semiconductor technologies. Recent research efforts have tried to integrate architecture and compiler solutions to employ power-gating mechanisms to reduce leakage power. This approach is to have compilers perform data-flow analysis and insert instructions at programs to shut down and wake up components whenever appropriate for power reductions. While this approach has been shown to be effective in our early studies [1, 2], there are concerns for the amount of power-control instructions being added to programs with the increasing amount of components equipped with power-gating control in a SoC design platform. In this poster, we have a quick review on our previous work and present a *Sink-N-Hoist* framework in the compiler solution to generate balanced scheduling of power-gating instructions. The main idea of the *Sink-N-Hoist* framework is to abate the problem of too many instructions being added with code motion techniques. The approach attempts to merge several power-gating instructions into one compound instruction by 'sinking' power-off instructions and 'hoisting' power-on instructions, i.e., postponing the issue of power-off instructions late and advancing the issue of power-on instructions early. This will result in profits mainly for code size, but also in performance and energy via grouping effects. For instance, a power-off instruction can be postponed for some cycles to be merged with other adjacent power-off instructions. Nevertheless, there should be a limitation on the number of cycles to be sank or hoisted since sinking or hoisting a power-gating instruction will cause more leakage dissipation. A cost model combining with architecture and power information is proposed to determine the feasibility. The proposed *Sink-N-Hoist Analysis* mainly consists of three phases: 1) the *Sinkable Analysis* and *Hoistable Analysis*, which compute the information of possible positions for each power-gating instruction, 2) the *Grouping-Off Analysis* and *Grouping-On Analysis*, which partition the turn-off and turn-on instructions into groups, and we can then use this information to group them by selecting emitting instructions, and 3) the power-gating instruction placement, which use the outcome of the former two analyses to determine how to place power-gating instructions. We evaluate the *Sink-N-Hoist* framework by incorporating our compiler analysis and scheduling policies into SUIF compiler tools and by simulating the energy consumptions on Wattch toolkits. The experimental results done with DSPstone benchmarks demonstrate that our mechanisms are effective in reducing the amount of power-gating instructions as well as producing power reductions over previous methods. It results in average 31.2% of reduction in the amount of power-gating instructions over the scheme without incorporating our Sink-N-Hoist framework for merging power-gating instructions. In fact, we further reduce the energy consumption in our framework. This is due to that the effect of a block version of power-gating instructions gives better power and performance effects than the pointwise version of power-gating instructions.

References

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